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A Background Calibration Technique and Self Testing Method for the Pipeline Analog to Digital Converter

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A Background Calibration Technique and Self Testing Method for the Pipeline Analog to Digital Converter

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To my parents.

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A Background Calibration Technique and Self Testing Method for the Pipeline Analog to Digital Converter

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Jae Ki Yoo, Ph.D.
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Analog to digital converters (ADCs) are the fundamental building blocks in highly integrated mixed-signal integrated circuits. Among several ADC architectures, the pipeline ADC is suitable for high sampling rate and high resolution, so it is widely used in many integrated applications such as, wireless transceivers, camcorders, portable video devices.

In this dissertation, a new digital background calibration technique with two redundant stages is proposed. Due to the redundant stages, calibration cycles can be scheduled to the pipeline stages during normal operation. The basic building blocks are the same as the building blocks in a normal pipeline ADC and no extra design time is required for dedicated calibration ADCs or DACs. The technique can calibrate all the gain errors, offset errors and the non-linearity errors of the ADC except for the front-end S/H. When compared

to the normal digital calibrated pipeline ADC, the digital hardware complexity is slightly increased. When compared to other background calibration techniques, it represents a compromise solution between with and without additional calibration converters. It is also suitable for converting high frequency input signals since there is nothing inherent causes in the algorithm that will degrade the performance for high input frequencies. A self-generated random signal based on the congruential mapping found in pipeline A/D converters is used as the test signal stimulus for histogram test. Almost no extra analog components are required for this random signal generation. The testing technique can be extended to in-field background verification if the converter is calibrated using skip-and-fill background calibration method.

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Chapter 1

Introduction

An analog-to-digital converter(ADC) is an electronic circuit that measures an analog signal such as a voltage that is proportional to a continuous physical quantity, such as temperature, pressure, or speed and converts it to a digital representation of the signal. It compares the analog input signal to a known reference signal and then produces a digital representation of the analog input. The output of an ADC is a digital binary code, which can represent only a finite number of values. Thus an ADC inherently introduces a quantization error, which is information that is lost. The more digital codes that the ADC can resolve, the more resolution it has and the less information lost due to the quantization error. Current digital applications create a need for high resolution and high-speed analog-to-digital converters. The pipeline ADC is a popular structure for high-speed data conversion with compact area and low power dissipation [1] so it is widely used in many integrated applications such as, wireless transceivers, camcorders, portable video devices, etc. Since CMOS technology provides high performance switches and accurate capacitor ratios, switched-capacitor circuits play fundamental role in ADCs. However, the trend of realization of analog and digital circuits on a chip requires scaling down the supply voltage of the analog circuits to match that of the digital cir-

cuits. This makes it difficult to design switched-capacitor circuits. Traditional pipeline converters have required high gain operational amplifiers and good capacitor matching. Low voltage circuits, which are used to reduce the power consumption have difficulty in the design of high performance analog parts, so the maximum gain of single stage operational amplifiers are decreasing, but the digital calibration technique can compensate the analog performance [22].

Usually in the absence of calibration or trimming, the pipeline ADC is generally limited to approximately 10-12 bit resolution. In order to achieve high performance, calibration techniques have been used and the importance of calibration is increasing, because it may be useful in even low-performance converters that are implemented with reduced technology, so calibration is an active research topic [2][3][4]. With calibration, another issue about the ADC manufacturing is the testing problem. In volume production, the testing cost remains a significant part of the price of manufacturing ADCs. Built-In Self-Test (BIST) is important, because BIST may reduce the cost of production test and offers in-field verification. Thus BIST provide a promising approach to automate mixed signal test generation [5]. Measurements are performed on chip, so this technique can reduce the cost of testing and does not significantly affect the hardware complexity. The histogram test is a popular ADC testing method, which gives much information about the characteristics of the converter [6][7]. The histogram test is based on a statistical analysis of how many times each digital code word appears on the output of ADC, when an analog input is applied whose amplitude distribution is known. Ramp and sinusoid

input signals are popular testing signals, but the generation of an exact high frequency ramp function is a difficult problem. In this dissertation two redundant stages are inserted into the conventional pipeline ADC architecture. Using these redundant stages, calibration and normal conversion can be overlapped to operate at the same time. Testing of the ADC is done using INL and DNL tests with the random signal method. This method utilizes a random input signal, that is self generated from the last pipeline stage of the ADC as the input stimulus for testing. Unlike the traditional ramp input or sinusoidal input histogram test, this method does not require any precise external signal sources.

Thus this dissertation presents methods to improve pipeline analog to digital converters, these methods including self calibration and random input built in testing can perform calibration and testing during normal ADC operation. These methods can increase the performance of pipeline ADC and can be performed in the background.

1.1 Dissertation Overview

High-speed analog-to-digital converters, which serve as bridges situated between analog signals and digital signals, play an important role in many digital signal-processing systems. The applications of ADCs include experimental equipment such as digital oscilloscopes, digital instruments and consumer products such as digital televisions and digital cameras. This dissertation addresses the architecture of pipeline analog-to-digital converters.

Chapter 2 presents some preliminary information that is needed to understand the rest of the dissertation. It includes a description of various architectures for analog-to-digital converters and a comparison of several ADCs. The characteristics of ADCs such as Differential Non Lineality Error(DNL) and Integral Non Linearlity Error(INL) are explained in this chapter.

Chapter 3 describes a proposed calibration technique using two redundant stages. In this architecture, two redundant pipeline stages are added to the conventional pipeline ADC such that calibration cycles can be performed during normal operation. Compared to other background calibration techniques, the proposed technique calibrates the gain errors, the offset errors and the non-linearity errors of the ADC. This chapter also describes a new approach for Built-In Self-Test (BIST) of pipeline ADCs that can measure the differential non-linearity (DNL) and integral non-linearity (INL) of the converter. This method utilizes a random input signal self generated from the pipeline ADC as the input stimulus for testing. It also includes behavior simulation results obtained using Matlab.

In Chapter 4, basic circuits for implementing pipeline ADCs like switch blocks, sample/hold blocks and general techniques for the low-voltage switched-capacitor circuits such as boostrapping switches, comparators, and their advantages and disadvantages are described. A basic 1.5 bit/stage architecture, a very common block for the pipeline ADC, is also explained. Simulation results for these blocks are also given in this chapter.

In Chapter 5, the operational amplifier, forming the core of the switched

capacitor circuit is described in detail, it is the most critical block of a pipeline stage. The resolution and speed of the whole ADC is usually determined by the characteristics of the operational amplifier. In general, the amplifier's open loop gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximum clock frequency. In order to get high gain, a gain boosting operational amplifier is used here. Simulation results of this opamp are described in this chapter.

Chapter 6 concludes this dissertation and gives some suggestions for future research.

Chapter 2

Basic Characteristics of Analog-to-Digital Converters

Modern analog to digital converters are divided into two different categories, Nyquist-rate ADCs [31], and oversampled ADCs. Nyquist-rate ADCs produce a series of output codes in which each code corresponds directly with one sample of the analog input signal. Oversampled ADCs sample an analog input at a much higher rate than the Nyquist-rate of the input signal and, obtain the desired output code by filtering out quantization noise that is outside of the signal bandwidth. Flash, successive approximation, and pipeline ADCs are Nyquist-rate type [27]. Sigma-delta ADCs belong to the oversampled ADC category. Each ADC structure has its own merits and drawbacks as discussed in the following sections.

2.1 Flash Analog-to-Digital Converter

Flash analog-to-digital converters, also known as parallel ADCs, are made by cascading high-speed comparators as shown on Figure 2.1. Flash ADCs are ideal for applications requiring very large bandwidth, however, they typically consume more power than other ADC architectures and are generally

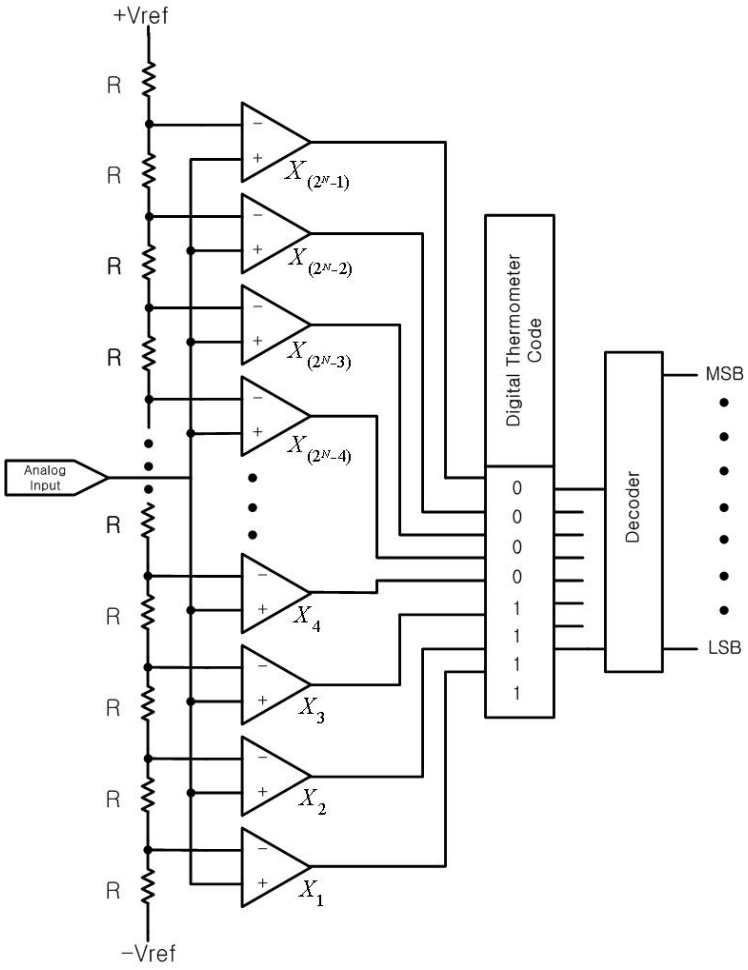


Figure 2.1: Flash ADC Architecture.

limited to 8-10 bits resolution [30]. As shown on Figure 2.1, a typical N-bit flash ADC employs $2^N - 1$ comparators, with 2^N matched resistors to provide a reference voltage for each comparator [33].

Each comparator represents 1 LSB and produces a '1' when its analog input voltage is higher than the reference voltage which is applied to it, oth-

erwise, the comparator output is '0.' If the analog input is between V_{X4} and V_{X5} , comparators X_1 through X_4 produce '1's and the remaining comparators produce '0's, the point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels, this output pattern is frequently called 'a thermometer code' since the height of the '1's rises and falls with the input voltages.

These comparators are typically a cascade of wideband low gain stages, they are low gain because at high frequencies, it is difficult to obtain both wide bandwidth and high gain, they are designed for low voltage offset, such that the input offset of each comparator is smaller than a LSB of the ADC, otherwise, the comparator's offset could falsely trip the comparator, resulting in 'bubbles' in the thermometer code [36]. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a '1' or a '0.' The result is subsequently converted to a binary output by an encoder. The principal advantage of the flash architecture is high throughput rate. The conversion of each sample takes only one single clock period. Many issues limit the utility of this approach for resolution above 8 bits, the exponential growth of the input capacitance, the power dissipation and the area are critical drawbacks. Furthermore the offset of the comparators, the feed through of the analog input to the resistor ladder, the slew-dependent comparator delay and bubbles in the thermometer code degrade the static and dynamic performance substantially [36][37].

2.2 Successive-Approximation-Register Analog-to-Digital Converter

Successive-approximation-register (SAR) ADCs are suitable for medium to high resolution applications [35]. SAR ADCs provide up to 5MSPS with resolutions from 8 to 16 bits. This combination makes them ideal for a wide variety of applications, such as portable instruments, pen digitizers, industrial controls. The SAR ADC basically implements a binary search algorithm, the basic architecture is quite simple as shown in Figure 2.2. The analog input voltage V_{in} is held on a sample/hold, to implement the binary search algorithm, the N-bit register is first set to mid scale, this forces the DAC output V_{DAC} to be $V_{ref}/2$, where V_{ref} is the reference voltage provided to the ADC.

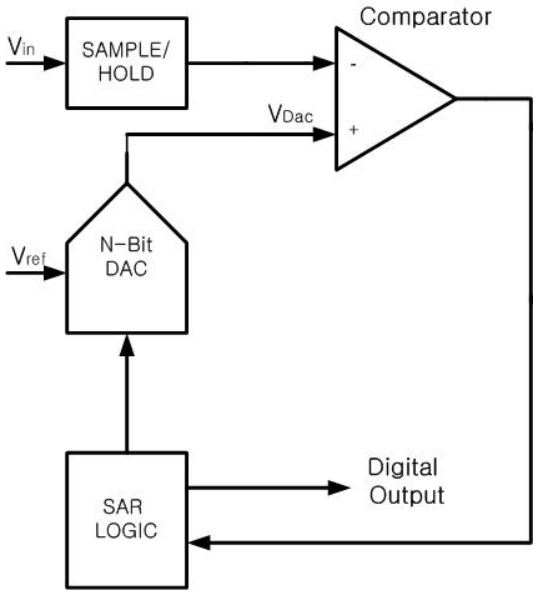


Figure 2.2: N-bit SAR ADC Architecture.

A comparison is then performed to determine V_{in}, if is less than or greater than V_{DAC}. If V_{in} is greater than V_{DAC}, the comparator output is a logic 'high' or '1' and the MSB of the N-bit register remains at '1'. Conversely, if V_{in} is less than V_{DAC}, the comparator output is a logic 'low' and the MSB of the register is cleared to logic '0'. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete, and the $N - bit$ digital word is available in the register.

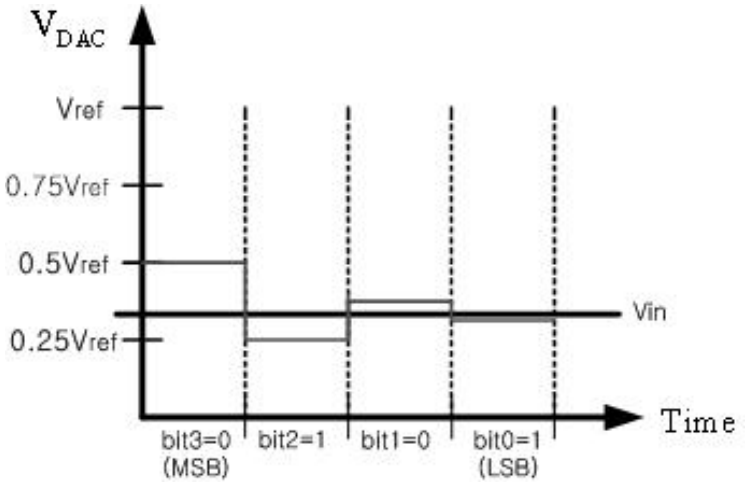


Figure 2.3: SAR Operation (4-bit ADC example).

Figure 2.3 shows an example of a 4-bit conversion. The y-axis represents the DAC output voltage. In the example, the first comparison shows that $V_{in} < V_{DAC}$. Thus, bit 3 is set to '0'. The DAC is then set to 0100_2 and the second comparison is performed. Since $V_{in} > V_{DAC}$, bit 2 remains at '1.' The DAC is then set to 0110_2, and the third comparison is performed.

Bit 1 is set to '0', and the DAC is then set to 0101_2 for the final comparison. Finally, bit 0 remains at '1' because $V_{in} > V_{DAC}$. Notice that four comparison periods are required for a 4-bit ADC. Generally speaking, an $N - bit$ SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. One other feature of SAR ADCs is that power dissipation scales with the sample rate, unlike flash or pipeline ADCs, which usually have constant power dissipation versus sample rate [35]. This makes the SAR ADC's especially useful in low-power applications or applications where the data acquisition is not continuous.

2.3 Sigma-Delta Analog-to-Digital Converter

Sigma-Delta ADCs are popular for high-resolution audio rate applications such as mobile telephones, digital audio, and ADSL. 20-bit ADCs have been reported without the need for any trimming [38]. A sigma-delta ADC combines a modulator with a high rate decimating filter. It can be high resolution by using a high oversampling ratio, but recently some high-bandwidth sigma-delta-type converters have reached a bandwidth of 1MHz to 2MHz with 12 to 16 bits of resolution. These are usually very highorder sigma-delta modulators incorporating a multi-bit ADC and multi-bit feedback DAC, and the main applications of these sigma-delta converters are in ADSL [39][25].

The structure of the basic sigma-delta converter is shown in Figure 2.4. The modulator consists of an integrator and a comparator, with a 1-bit DAC in a feedback loop, the internal DAC is simply a switch that connects the

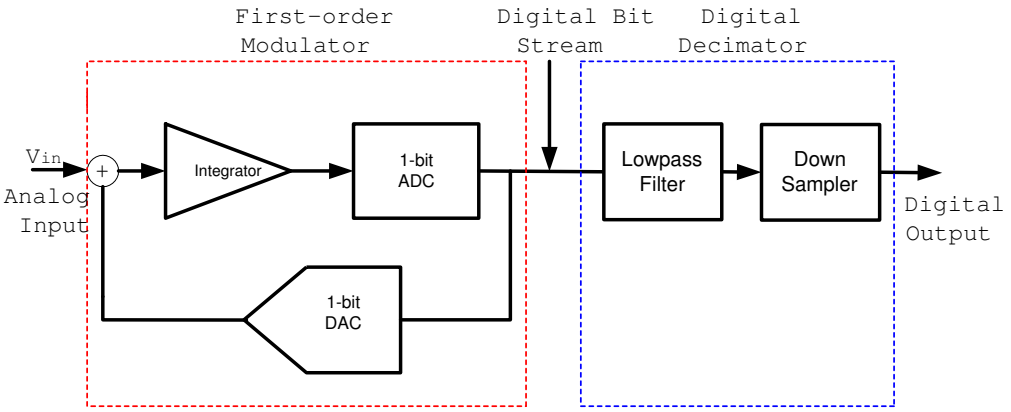


Figure 2.4: The Sigma-Delta Over Sampling ADC Architecture.

comparator input to a positive or negative reference voltage The modulator produces an output that consists of a stream of digital '1's and '0's, where the percentage of '1's varies in direct proportion to the analog input. The digital decimator that follows performs both digital filtering and down-sampling of the 1-bit input data stream. The sigma-delta ADC also includes a clock unit that provides proper timing for the modulator and digital decimator [40]. A significant problem with the sigma-delta converter, resulting directly from its nonlinear nature and feedback, is the presence of 'tone' components in the output in response to DC inputs, or even small amplitude sinusoidal inputs. Clearly, these tones are highly undesirable in audio and speech applications, for this reason, higher than second order modulators are used to alleviate some of the idle tone problem. In general, for an N order modulator every doubling of the oversampling ratio provides an additional $6N + 3dB$ of SNR. Higher order modulation can also be achieved by cascading several lower order stages. This

avoids problems with stability, while maintaining the advantages with respect to SNR and limit cycles. Fourth order modulators of two cascaded second-order stages are common. There are also architectures which employ multibit quantizers. For example, in a second order modulator, each additional bit in the quantizer will results in a SNR improvement of about $6dB$.

2.4 Pipeline Analog-to-Digital Converter

The pipeline analog-to-digital converter has become the most popular ADC architecture for sampling rates from a few MSPS up to 100 MSPS, with resolutions from 8 bits to 16 bits. These kinds of resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic biomedical imaging, digital receiver, digital video for high density TV, ADSL, cable modem, and fast Ethernet. Lower-sampling-rate applications are still the domain of the SAR and sigma-delta ADCs. The highest sampling rates are still obtained using flash ADCs. However, various forms of the pipeline ADCs have developed greatly in speed, resolution, dynamic performance, and low power in recent research [18][42][41].

Figure 2.5 shows a block diagram of a 12-bit pipeline ADC. The analog input V_{in} is first sampled and held by a sample-and-hold circuit, while the flash ADC in stage one quantizes it to 3 bits. The 3 bit output is then fed to a 3 bit DAC, and the analog output is subtracted from the input. This residue is then multiplied up by a gain factor and fed to the next stage. This gained-up residue continues through the pipeline, providing 3 bits per stage

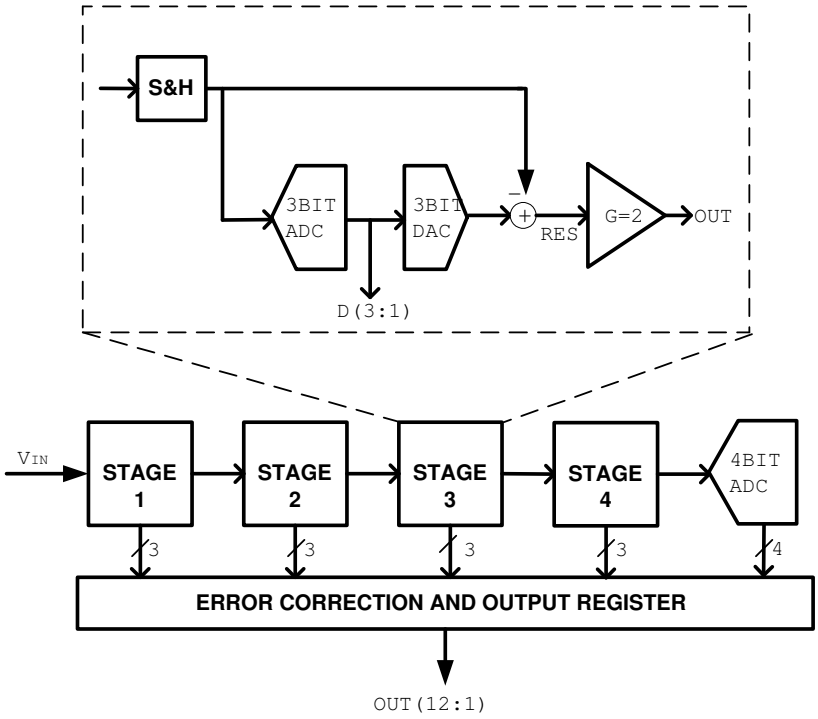


Figure 2.5: Pipeline ADC Architecture.

until it reaches the 4 bit flash ADC, which resolves the last 4 LSBs. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that as soon as a certain stage finishes processing a sample, determining the bits and passing the residue to the next stage, it can start processing the next sample due to the sample-and-hold embedded within each stage. This pipelining action accounts for the high throughput [29].

In a SAR ADC, the bits are decided by a single high-speed, high-accuracy comparator bit by bit, from the MSB down to the LSB, by comparing the analog input with a DAC, whose output is updated by previously decided bits and successively approximates the analog input. This serial nature of SAR limits its operating speed to no more than a few MSPS, and still slower for very high resolutions. A pipeline ADC, however, employs a parallel structure in which each stage works on one to a few bits concurrently. Although there is only one comparator in a SAR, this comparator has to be fast and as accurate as the ADC itself. In contrast, none of the comparators inside a pipeline ADC needs this kind of accuracy. However, a pipeline ADC generally takes up significantly more silicon area than a SAR of equivalent resolution. Fast flash ADCs exist with sampling rates as high as 1.5 GSPS, but it is much harder to find a 12-bit flash. This is simply because in a flash ADC, the number of comparators is 256 for an 8 bit converter and the number goes up by a factor of 2 for every extra bit of resolution, and at the same time each comparator has to be twice as accurate.

In a pipeline ADC, however, to a first order the complexity only increases linearly with the resolution, not exponentially. At sampling rates obtainable by both a pipeline and a flash, a pipeline ADC tends to have much lower power consumption than a flash [32]. So the pipeline ADC is the architecture of choice for sampling rates from a few MSPS up to 100 MSPS. They are very useful for a wide range of applications, most notably in the digital communication area, where a converter's dynamic performance is often

more important than traditional DC specifications like DNL and INL. Table 2.1 provide a comparison of the several various high performance ADCs and Figure 2.6 illustrates the bandwidth and sampling rate of the ADCs.

Table 2.1: Major Analog-to-Digital Converter Techniques.

Architecture	Resolution	Speed	Advantage
Flash	8 Bits	250 Msps - 1Gsps	- Extremely Fast - High Speed Rate - Highest Power Consumption - Large Die Size - High Input Capacitance
SAR	10-16 Bits	75 Ksps - 250Ksps	- High Resolution and Accuracy - Few External Components - Low Power COnsumption - Low Sample Rate
Sigma-Delta	16 Bits	200 Ksps	- High Resolution - High Input Bandwidth - Both analog and Digital Circuit on Same Chip - External S/H - Low Sample Rate
Pipeline	12-16 Bits	1 Msps-100 Msps	- High Sample Rate - Low Power Consumption - Digital Error Correction

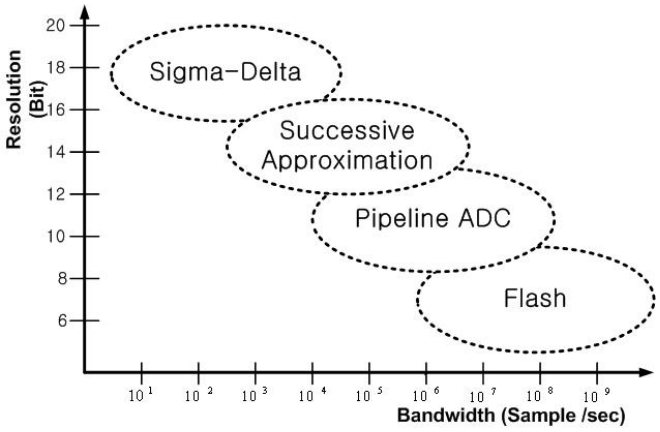


Figure 2.6: Basic ADC Comparison with Resolution and Bandwidth

2.5 Analog-to-Digital Converter Performance

An ADC with a 12-bit-resolution does not necessarily have 12 bit accuracy, because the converter sometimes exhibits lower performance than expected due to non linear parameters. ADC characteristics are helpful to select the appropriate ADC architecture. Each component in a system will have associated errors, so the goal of the converter specification is to keep the total error below a certain value. Often the ADC is the key component in the signal path, so care is required to select a suitable device. The accuracy of the ADC is dependent on several key specifications, which include differential non linearity errors (DNL), integral non linearity errors (INL), offset and gain errors, and the accuracy of the voltage reference, temperature effects. If 0.1% or 10 bits of accuracy ($1/2^{10}$) is needed, then it makes sense to choose a converter with greater resolution than this. If a 12 bit converter is selected, it may be assumed to be adequate, but without reviewing the specifications, there is no guarantee of 12 bit performance. For example, a 12 bit ADC with 4 LSBs of integral non linearity error gives only 10 bits of accuracy at best (assuming the offset and gain errors have been calibrated). ADC performance can be defined in two different ways, static performance and dynamic performance. Dynamic performance is especially important for telecommunication systems [43][20].

2.5.1 Differential Non Linearity (DNL)

The differential non linearity (DNL) error is defined as the difference between an actual step width and the ideal value of 1 LSB. For an ideal ADC,

the differential non linearity coincides with 0 LSB, and the transition values are spaced exactly 1 LSB apart. A DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases or remains constant, thereby avoiding sign changes in the slope of the transfer curve. DNL error is defined as follows,

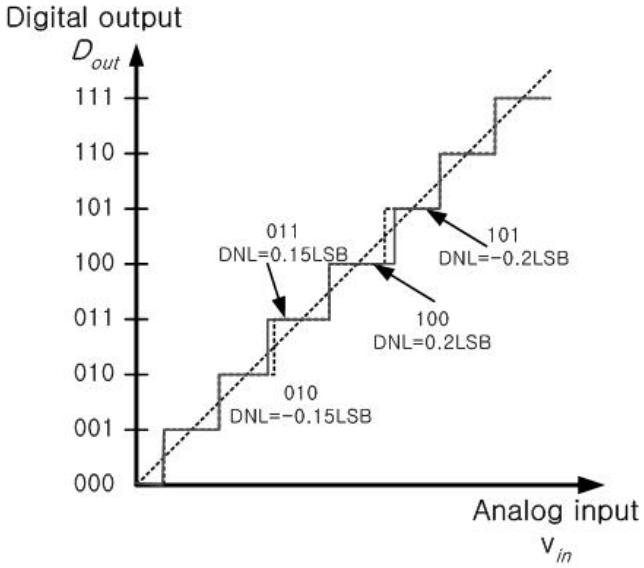
$$DNL = \left[\frac{(V_{D+1} - V_D)}{V_{LSB}} - 1 \right], \quad \text{where} \quad 0 < D < 2^N - 1 \tag{2.1}$$

With a DNL error less than 1 LSB, the device is guaranteed to have no missing code as shown in Figure 2.7(a), and with a DNL value -1, the device has missing codes as shown in the Figure 2.7(b).

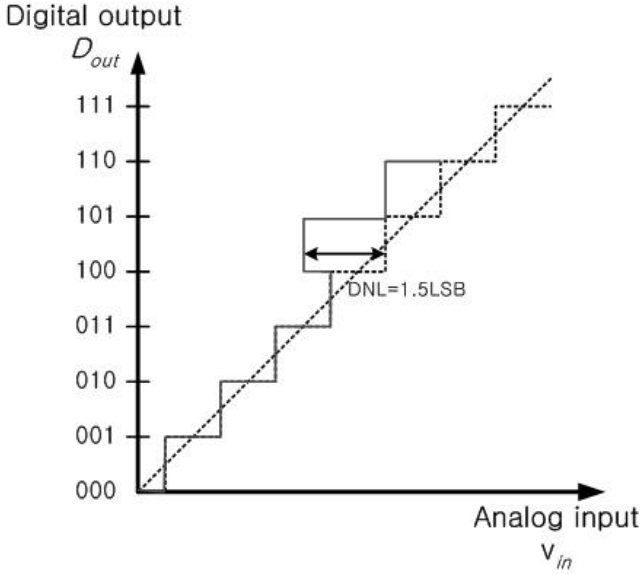
2.5.2 Integral Non Linearity (INL)

INL is defined as the integral of the DNL errors, so good INL guarantees good DNL. INL error is described as the deviation, in LSB or percent of full-scale range, of an actual transfer function from a straight line. An INL error of ± 2 LSB in a 12 bit ADC means the maximum non linearity error may be off by 2/4096 or 0.05%. The INL error magnitude then depends directly on the position chosen for this straight line. Two common methods "best straight-line INL" and "end-point INL" are popular to measure the INL errors as shown in Figure 2.8.

Best straight-line INL provides information about the offset and gain error plus the position of the transfer function. It can be determined from the



(a)



(b)

Figure 2.7: Symbol (a) DNL error: no missing codes (b) missing codes.

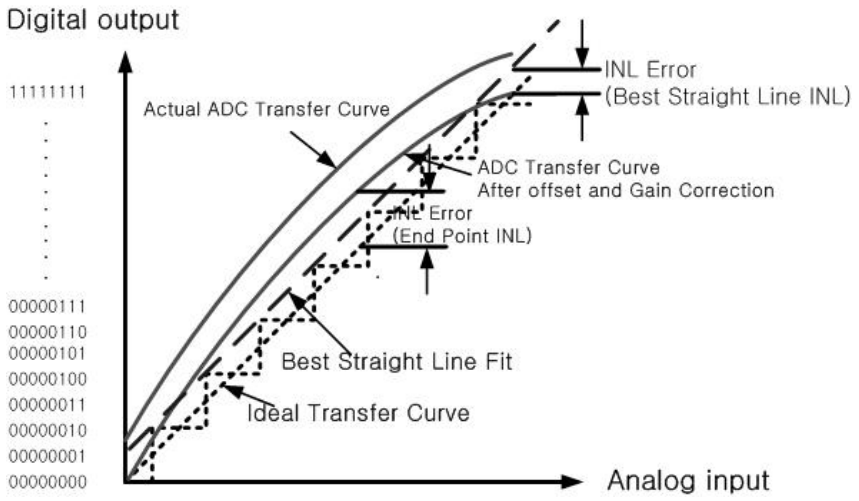


Figure 2.8: Best Straight-Line and End-Point Fit.

least mean square (LMS) method, and this line is the closest approximation to the ADC's actual transfer function. The exact position of the line is not clearly defined, but this approach yields the best repeatability [21], and it serves as a true representation of linearity. End-point INL passes the straight line through end points of the converter's transfer function, thereby defining a precise position for the line. Thus, the straight line for an N-bit ADC is defined by its zero and its full scale outputs or its full scale negative and full scale positive outputs.

The best straight-line approach is generally preferred, because it produces better results. The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows

$$INL = \left[\frac{(V_D - V_{Zero})}{V_{LSB}} - D \right], \quad \text{where} \quad 0 < D < 2^N - 1 \tag{2.2}$$

$$V_{LSB} = \frac{V_{FullScale} - V_{Zero}}{2^N - 1} \tag{2.3}$$

V_D is the analog value represented by the digital output code D, N is the ADC's resolution, V_{ZERO} is the minimum analog input corresponding to an all-zero output code, and V_{LSB} is the ideal spacing for two adjacent output codes.

2.5.3 Sources of Errors in Pipeline Analog-to-Digital Converters

There are three major error sources in a pipeline ADC. The first one is the gain error which is introduced by finite opamp gain. This can be removed by adjusting the gain of the opamp. The second error is the offset of the opamp. This error requires some special techniques to remove. The last error is from capacitor mismatch and this can be cancelled by digital calibration techniques [21].

The gain error is defined as the full-scale error minus the offset error. Full-scale error is measured at the last ADC transition on the transfer-function curve and compared against the ideal ADC transfer function. Gain error is easily corrected with a linear function $y = (m1/m2)(x)$, where m1 is the slope of the ideal transfer function and m2 is the slope of the measured transfer function (Figure 2.9). In order to remove the offset error the x and y axes of the transfer function are shifted so that the negative full-scale point aligns with the zero point of a system. With this technique, the offset error is removed and then the gain error is removed by rotating the transfer function about the

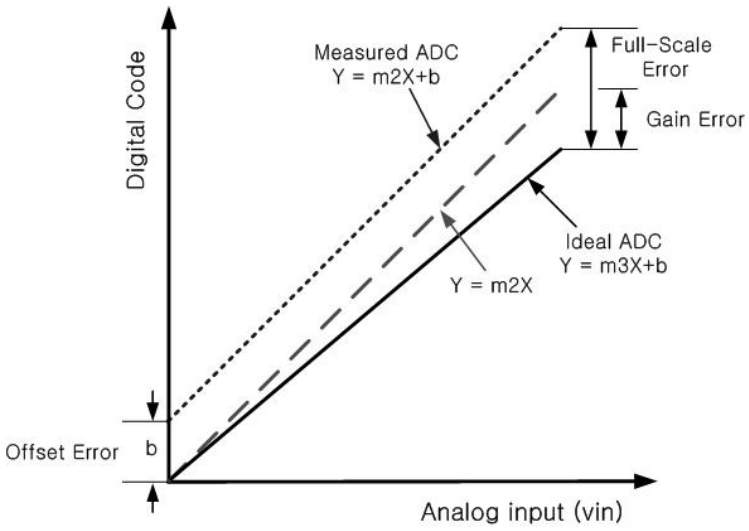


Figure 2.9: Offset, Gain, and Full-Scale Errors.

'new' zero point. The gain-error specification may or may not include errors contributed by the ADC's voltage reference. In the electrical specifications, it is important to check the conditions to see how gain error is tested and to determine whether it is performed with an internal or external reference. Typically, the gain error is much worse when an on-chip reference is used [16]. Figure 2.10 shows the effect of finite opamp gain error. Because of finite opamp gain, there is an error voltage at the input of opamp. From Equation (2.6), the error term ($A_0\beta$) makes the slope of the residue plot less than two or more than two, so the residue voltage may be less than or greater than the full range of the converter.

$$(C_s + C_f) \cdot V_{in} = C_s(0 + \frac{V_{out}}{A_0}) + C_f(V_{out} + \frac{V_{out}}{A_0}) \tag{2.4}$$

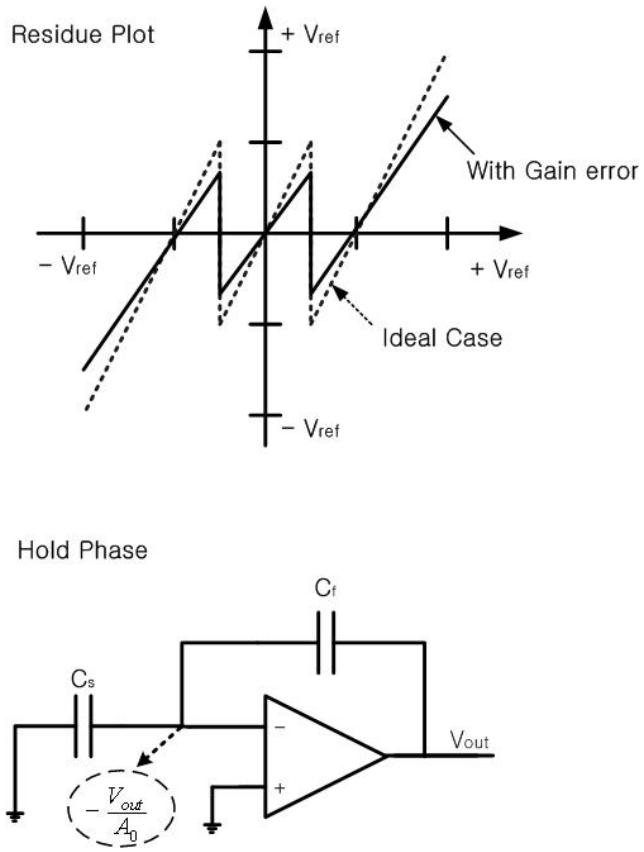


Figure 2.10: Residue Plot of a 1.5 bit Pipeline Stage with Finite Gain Error.

$$V_{out} = \frac{C_f + C_s}{C_f + \frac{1}{A_0(C_s+C_f)}} V_{in} = (1 + \frac{C_s}{C_f}) \frac{1}{1 + \frac{1}{A_o \beta}} V_{in} \tag{2.5}$$

$$= (1 + \frac{C_s}{C_f})(1 - \frac{1}{A_0 \beta}) V_{in} \tag{2.6}$$

As shown in Figure 2.11, the offset of opamp introduces a constant error, or a shift, at the output of pipeline stage. From Equation (2.7), this

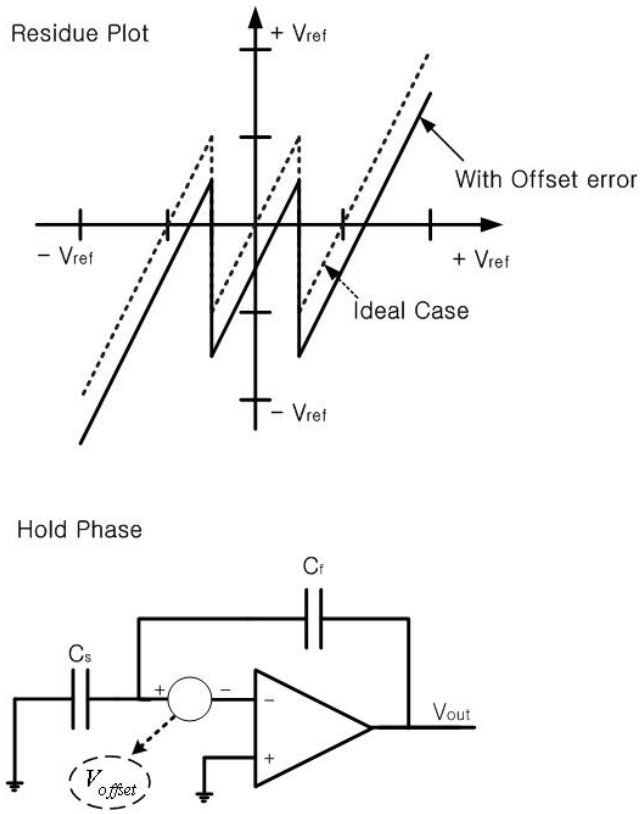


Figure 2.11: Residue Plot of a 1.5 bit Pipeline Stage with Operational Amplifier Offset.

error voltage is represented by Equation (2.8)

$$0 = C_s(0 - V_{offset}) + C_f(V_{error} - V_{offset}) \tag{2.7}$$

$$V_{error} = (1 + \frac{Cs}{Cf})V_{offset} \tag{2.8}$$

To reduce the offset error, the input transistors are often kept quite big, which usually takes a large area. If a 1.5 bit stage is used in the pipeline,

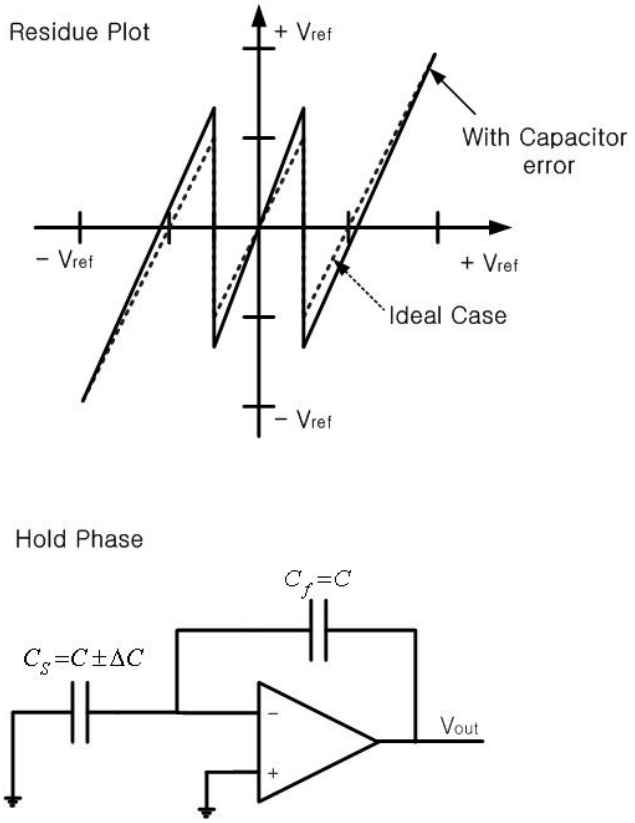


Figure 2.12: Residue Plot of a 1.5 bit Pipeline Stage with Capacitor Mismatch.

this error will be corrected by the later stages. The major cause of gain and offset error is capacitor mismatch, so matched capacitors or precision capacitor ratios have been used extensively for many years. There are several mismatch error sources in MOS capacitors. The major error source consists of long range, gradient related system errors, which are strongly correlated for all capacitors on the same chip. These can be kept to a minimum by using unit capacitor layout techniques with a common centroid geometry [44][42]. Figure 2.12 shows the effect of capacitor mismatch. Because of process variations,

capacitor mismatches always exist. Capacitor mismatch changes the slope of the residue plot to a value different than two.

$$V_{out} = (1 + \frac{Cs}{Cf})V_{in} = (2 \pm \frac{\Delta C}{C})V_{in} \tag{2.9}$$

2.6 Dynamic Performance

Dynamic performance includes dynamic linearity, noise and distortion. The following measures are used to characterize the dynamic performance of an ADC. Signal-to-Noise Ratio (SNR) is the ratio of the signal power to the total noise power at the output of ADC with full-scale sinusoidal input. It can be calculated by Equation (2.10), with an N-point FFT of a signal [22].

$$SNR(dB) = Signal\ Peak(dB) - Noise\ Floor(dB) - 10\ logN \tag{2.10}$$

$$SNR(dB) = 6.02N + 1.76dB \tag{2.11}$$

Signal-to-Noise + Distortion Ratio (SNDR) is the ratio of the signal power to the total noise and harmonic power at the output of ADC with full-scale sinusoidal input. Dynamic Range (DR) is the range of input signal amplitudes within which the desired output can be obtained, that is, it is the input power range for which the SNR is greater than 0 dB. Spurious Free Dynamic Range (SFDR) is the ratio of the signal power to the largest spurious component within a certain frequency band. It is important for telecommunication applications. The Effective Number Of Bits (ENOB) is calculated with

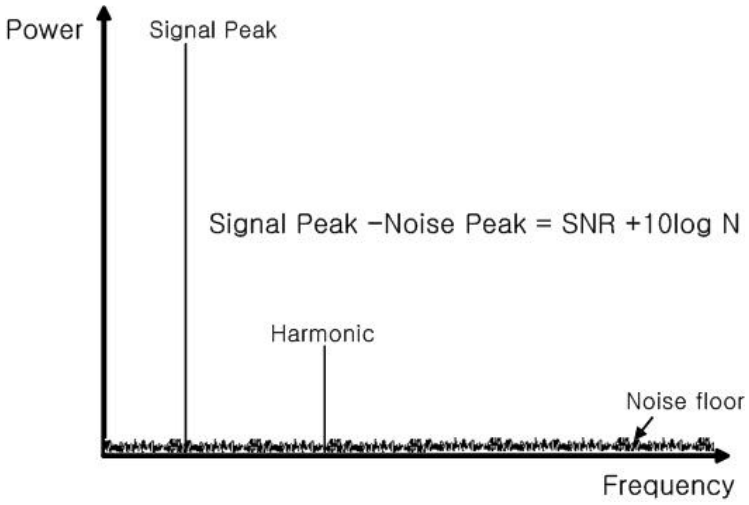


Figure 2.13: Procedure for Computing SNR from an N point FFT.

the following equation

$$ENOB = \frac{(SNDR - 1.76)dB}{6.02dB} \tag{2.12}$$

Chapter 3

Digital Calibration and Testing Methods

A new digital background calibration technique for pipeline ADC is proposed in this dissertation. In this architecture, two redundant pipeline stages are added to the ADC, such that calibration cycles can be performed during normal operations. Compared to other background calibration techniques, the proposed technique calibrates the gain errors, the offset errors and the non-linearity errors of the ADC. It is not necessary to design dedicated separate ADCs or DACs for calibration. It also provides no degradation in performance for high frequency input signals and the complexity of the digital hardware is relatively simple. This chapter also describes a new approach for Built-In Self-Test (BIST) of pipeline ADCs that can measure the differential non-linearity (DNL) and integral non-linearity (INL) of the converter. This method utilizes a random input signal self generated from the pipeline ADC as the input stimulus for testing. Unlike the traditional ramp input or sinusoidal input histogram test, this method does not require any precise external input signal sources. It provides a low hardware cost solution for in-field verification since no extra precise analog circuits for signal generation are required. In addition, it is also possible to extend this concept to background self-testing.

3.1 Digital Calibration Techniques

Digital processing techniques used in communication and video systems have been developed rapidly. As a result, there is a need for high performance ADCs. Pipeline ADCs using switched-capacitor techniques are popular structures for high speed and high resolution data converters since they provide the advantages of low die area and low power consumption [3]. Traditional pipeline ADCs rely on good capacitor matching for good linearity. Without any calibration or trimming, the accuracy of the ADC is generally limited to about 10 bits of accuracy.

To achieve higher accuracy, a variety of calibration techniques have been developed(e.g., [2] [3]). However, interrupting the ADC normal operation for performing calibration steps is required. In some applications, these calibration steps may not be allowed and the calibration steps have to be performed in the background. Furthermore, any miscalibration or sudden environmental changes such as temperature changes may cause the calibrated values to change. As a result, the accuracy of the ADC may decrease after calibration, to overcome this disadvantage background calibration techniques have been proposed. In [4], a separate ADC is used in the background for measuring component errors for calibration. Other techniques use a dedicated DAC for creating analog values in order to measure gain and offset errors [45] [46]. Another way is to duplicate the ADC such that one of the ADCs is in calibration mode while the other one is used in normal operation. When the first converter is not being calibrated it can be used in parallel with the second

converter with comparison of the outputs to detect errors. To avoid any extra ADCs or DACs, the skip-and-fill method was proposed [47]. In this case, one of the input samples to the ADC is skipped every fixed number of clock cycles such that calibration can be performed in these cycles. The missing input samples are then obtained by digital interpolation from other digital outputs. Due to these operations, the performance of the ADC for high frequency input signals is degraded.

In this dissertation, a new digital background calibration technique based on adding redundant pipeline stages is proposed. This technique represents a compromise that is less complex than the use of extra converters for calibration. The calibration technique described in [3] is extended for using the proposed technique. When the ADC is in calibration mode, the last stage output is connected to the input of the first stage as shown in Figure 3.1. The last stage output is forced to one of the DAC output levels by forcing the input of the last stage to zero and setting the digital DAC input of the last stage to one of the output levels. The last stage output is then measured by the remaining stages and the result is then updated and forms the corresponding weight in the digital memory. This procedure is repeated until all the DAC output levels of the last stage are calibrated. Afterwards, the DAC output levels of the second last stage are calibrated using the remaining stages and the corresponding weights are updated in the digital memory. The above process is repeated until the first stage is calibrated. The weights obtained from the above procedure are then used for calculating the corrected digital

outputs during normal operation. The detailed calculation of the weights can be found in [3]. When the above calibration process is repeated the accuracy of the ADC can be improved further.

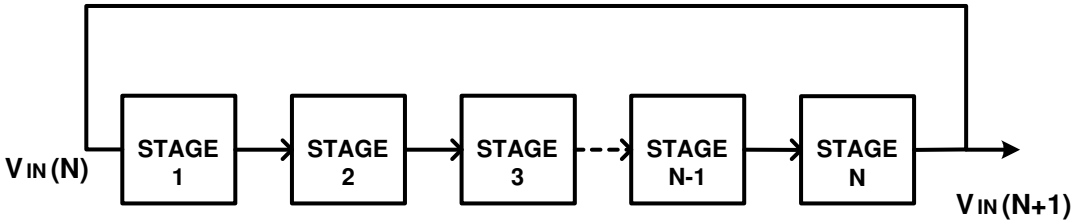


Figure 3.1: Block Diagram of ADC Calibration.

The above calibration [26] technique was not intended for background calibration since when a particular stage is used for calibration, it could not be used for normal operation. To overcome this problem, two redundant stages are addeded to the ADC such that there is always one stage free for calibration in every clock phase ϕ_1 or ϕ_2. The scheduling of operations for each stage is discussed in the next section.

3.2 Proposed Digital Background Calibration Technique

A pipeline stage is usually implemented based on switched-capacitor techniques. Furthermore, in a practical design, the odd stages of the pipeline will have clock phase ϕ_1 as the sampling phase and a second clock phase $\phi 2$ as the evaluating phase. For even stages, the operations for the different clock phases will be vice versa. Due to capacitor mismatch error and offset errors on the opamps and comparators the accuracy of the ADC is degraded. As an

illustration, for a 1.5 bit per stage architecture, the output of stage i, V_{i+1}, can be written as

$$V_{i+1} = (2 + \alpha_i)V_i - D_i(1 + \alpha_i)V_{ref} + o_{ai} \tag{3.1}$$

$$D_i = \begin{cases} -1 & V_i < -0.25V_{ref} < o_{ci_2} \\ 0 & -0.25V_{ref} + o_{ci_2} < V_i < 0.25V_{ref} + o_{ci_1} \\ 1 & V_i > -0.25V_{ref} + o_{ci_1} \end{cases}$$

Where o_{ai} is the offset due to the opamp, o_{ci1} and o_{ci2} are the comparator offset errors and α_i is the capacitor mismatch error. When $|o_{ci1}|$ and $|o_{ci2}|$ are smaller than $0.25V_{ref}$, they will not affect the final digital outputs of the ADC for this architecture. However, o_{ai} will produce an overall offset for the ADC and α_i will affect the amplifier gain and the DAC output levels of stage i. Hence, the linearity of the ADC will be affected. To correct for the non-linearity error of the ADC, digital calibration techniques have been proposed [2] [3].

In this dissertation, two redundant stages are added to the ADC such that digital calibration algorithm can be scheduled to different stages during normal operation. The ADC architecture of proposed digital background calibration is shown in Figure 3.2. The output of the front-end sample-and-hold (S/H) is multiplexed to different pipeline stages. The input to each stage can be selected either from the S/H output or from the output of the previous stage. The previous stage for the first stage is the last pipeline stage. Therefore, any stage can be the most significant bit (MSB) stage. Each stage can be selected for calibration operation by forcing the input to the DAC or for

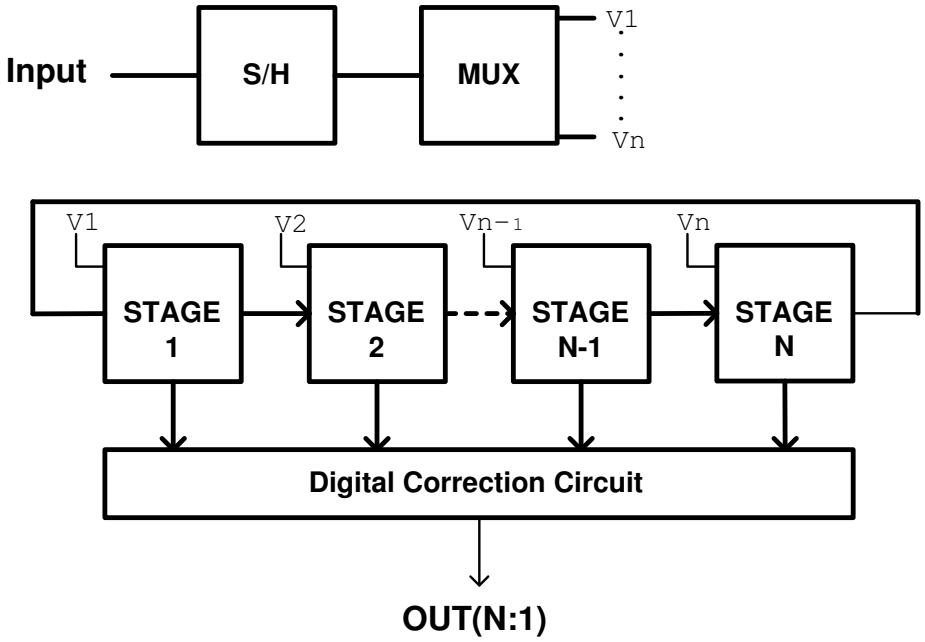


Figure 3.2: Block Diagram of the Proposed A/D Converter.

normal operation, which outputs the digital values and the analog residue for the input either from the S/H or from the previous stage. Table 3.1 illustrates the scheduling of operations for different stages at different clock phases. In this case, the ADC is assumed to consist of four stages plus two redundant stages. In the table, S_{ij} represents that this particular stage is producing the j-th bit (or j-th group of bits in a multi-bit per stage architecture) for the i-th input sample at the corresponding clock phase. C_{ij} represents that this particular stage is producing the j-th bit (or j-th group of bits) for the calibration of the i-th stage. According to this schedule, the output of the S/H in the first three clock cycles is connected to stage 1 and sampled at ϕ_2. The conversion

Table 3.1: Scheduling of Operations for Different Stages in the Background Calibrated ADC.

Cycle	Phase	1	2	3	4	5	6
1	ϕ_1	S_{11}					
	ϕ_2		S_{12}				
2	ϕ_1	S_{21}		S_{13}			
	ϕ_2		S_{21}		S_{14}		
3	ϕ_1	S_{31}		S_{23}		C_{41}	
	ϕ_2		S_{32}		S_{24}		C_{42}
4	ϕ_1	C_{43}		S_{33}		S_{41}	
	ϕ_2		C_{44}		S_{34}		S_{42}
5	ϕ_1	S_{43}				S_{51}	
	ϕ_2		S_{44}		C_{31}		S_{52}
6	ϕ_1	S_{53}		S_{61}		C_{32}	
	ϕ_2		S_{54}		S_{62}		C_{33}
7	ϕ_1	C_{34}		S_{71}		S_{63}	
	ϕ_2				S_{72}		S_{64}
8	ϕ_1	S_{81}		C_{21}		S_{73}	
	ϕ_2		S_{82}		C_{22}		S_{74}
9	ϕ_1	S_{91}		S_{83}		C_{23}	
	ϕ_2		S_{92}		S_{84}		C_{24}
10	ϕ_1			S_{93}		S_{101}	
	ϕ_2		C_{11}		S_{94}		S_{102}
11	ϕ_1	S_{103}		C_{12}		S_{111}	
	ϕ_2		S_{104}		C_{13}		S_{112}
12	ϕ_1	S_{113}		S_{121}		C_{11}	
	ϕ_2		S_{114}		S_{122}		
13	ϕ_1	C_{61}		S_{131}		S_{123}	
	ϕ_2		C_{62}		S_{132}		S_{124}
14	ϕ_1	S_{141}		C_{63}		S_{133}	
	ϕ_2		S_{142}		C_{64}		S_{134}
15	ϕ_1	S_{151}		S_{143}			
	ϕ_2		S_{152}		S_{144}		

of the LSB of the first input sample is completed at ϕ_2 of the second clock cycle by stage 4. Since, at this time, no residue voltage is needed from stage 4 for further conversion, the DAC inputs of stage 4 are forced for calibration and the output is sampled by stage 5, which is free at this time. The MSB of this calibration is obtained from stage 5 in the next clock phase. Notice that the third bit of the calibrated value for stage 4 is obtained from stage 1 at $\phi_1$in the fourth clock cycle. In order not to miss an input sample, stage 4 is used

for producing the MSB for the fourth input sample and therefore, the output of the S/H is connected to stage 4 at ϕ_2 in the third clock cycle. Similarly, as illustrated in Table 3.1, the calibration of each stage can be scheduled for each of the stages without missing any input samples.

In the original digital calibration algorithm in [3][14] the overall offset and gain error of the ADC are not calibrated. It only guaranties the linearity of the ADC. An extra calibration step is required for the overall offset and gain errors. However, in the above background calibration process, the MSB stages for the input signal are changed among different clock cycles. As a result, the offset and gain errors of the overall ADC will change between different clock cycles creating spurs at the output. To overcome this problem, the overall gain and offset errors for a particular stage configured as the MSB stage for the input signal can be measured in the calibration cycles that are scheduled for this stage. The overall gain and offset errors are measured by applying $\pm V_{ref}$ to the MSB stage and then correcting at the digital output.

In general, for an N stage (including two redundant stages) pipeline architecture, the MSB stage will shift to left two stages for every $(N-2)/2+1$ clock cycles. If each stage has M DAC levels, the number of clock cycles to complete the calibration of all stages once is

$$N \quad (M+1)(\tfrac{N-2}{2}+1) \tag{3.2}$$

The advantages of the proposed technique are that there is no extra design time required for designing a separate ADC or DAC for calibration and the

die area requirement is less than that of duplicating the entire pipeline ADC. In addition, the response to high frequency input signals is the same as that of the original pipeline ADC without redundant stages. In terms of hardware requirements, it is slightly more complex than a normal digital calibrated pipeline ADC due to the additional hardware for the permutation of the output bits to the right order and the additional storage requirements for the overall gain and offset errors of the $N/2$ possible MSB stages.

3.3 ADC Histogram Test

When a linear ramp input is used in histogram test, the Integral Non Linearity (INL) and the Differential Non Linearity (DNL) of the converter can be determined quite easily due to the uniform amplitude distribution of the ramp signal. The DNL is expressed by Equation (3.3), and the INL can be calculated using the DNL results with Equation (3.4) where $H(i)$ is the measured occurrence of code i and Hideal is the ideal occurrence. Furthermore, the error in measuring $DNL(i)$, can be expressed by Equation (3.5), a large value of H_{ideal} should be used to have an accurate measurement of DNL. For example, if a DNL accuracy better than 0.05LSB is required, H_{ideal} should be higher than 20.

$$DNL_i = \frac{H(i) - H_{ideal}}{H_{ideal}} \tag{3.3}$$

$$INL_i = \sum_{k=1}^{i} DNL(k) \tag{3.4}$$

$$\epsilon DNL(i) = \frac{\epsilon H(i)}{H_{ideal}} \tag{3.5}$$

The sinusoidal input histogram test is another popular method to measure ADC characteristics, compared to the ramp input, sinusoidal signals are easily and accurately generated with relatively simple circuits. Another reason to use the sinusoidal input histogram method is that it allows better characterization of the dynamic performance of the ADC. The linear ramp input histogram technique is basically a static test, but sometimes a test of the transition levels of converter is needed, leading to the use of a high frequency sinusoidal input signal. Sinusoids have a non-uniform distribution of voltages as shown Figure 3.3, so more code hits are expected at the upper and lower codes than at the center of the ADC's transfer curve, even when testing a perfect ADC. To get DNL accuracy better than 0.25 LSB, the total sample size needs to be almost 1.5 times larger than the number of samples required for the linear ramp input histogram test [6].

3.4 Proposed Self-testing Method

Statistically, a uniformly distributed random signal has the same amplitude distribution as a linear ramp signal. However, in order to guarantee that the random signal probabilaty density function is almost the same as that of ramp signal, H_i in Equation (3.5) will become large. When this is satisfied, a uniformly distributed random signal can be used as the input stimulus for testing the ADC. The next sections discuss the self-generation of uniformly

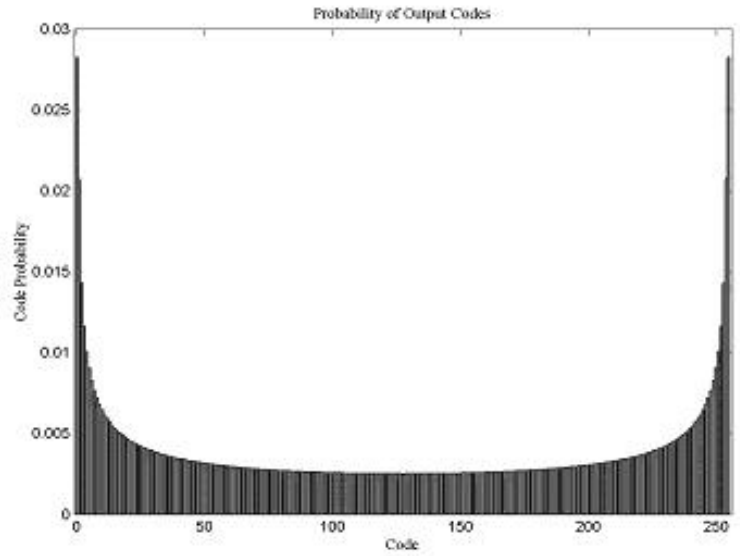


Figure 3.3: The Probability of Output Codes for the Sinusoidal Input Histogram Test.

distributed random signal in the pipeline ADC by first discussing the linear congruential random number generation method.

One of the most popular methods for generating pseudo random numbers in computer programming is the linear congruential mapping [21], this technique uses a method similar to folding schemes in chaotic maps. The general formula is given by

$$I_k = (I_{k-1} \times a + c) Mod M \tag{3.6}$$

The parameters a, c, and M are pre-selected integer constants. The multiplier is a, c is the increment, and M is the modulus. The quality of the generator is strongly dependent upon the choice of these constants. A good set of pa-

rameters causes the output of the random generator I_k to go through all the possible integers that are less than M. The above congruential mapping can be implemented using analog circuits [48] [49]. In fact, the basic operation of each stage in a pipeline ADC realizes one iteration of Equation (3.6) with all the mapping coefficients I_k, a, c and M being infinite resolution real numbers instead of integers. Therefore, by connecting the output of the last stage of the pipeline ADC back to the first stage as shown in Figure 3.4, the recursive operation in Equation (3.6) can be realized [50] except that the mapping coefficients in each iteration are slightly different between each stage due to mismatch and offset errors. An ideal simple 1-bit per stage pipeline ADC is equivalent to a congruential mapping with modulo 2. A similar technique for analog noise generation that is based on the Delta-Sigma structure has also been developed. The randomness of linear congrunetial mapping is also discussed in [51].

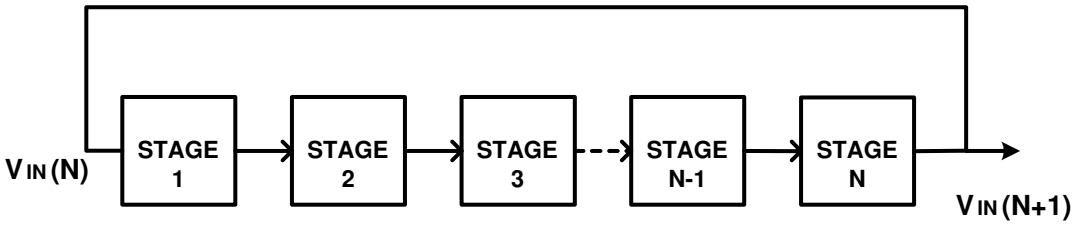


Figure 3.4: Block Diagram of Random Signal Generation.

Unlike the case of having the mapping coefficients being integer values, real mapping coefficients with slightly different values will not affect the randomness of the output. Furthermore any circuit noise will also help to

randomize the output values. However, the input range to each stage has to be bounded to avoid saturation in each stage. To illustrate the prevention of saturation, a 1.5 bit per stage architecture is used. The ideal transfer characteristic for each stage is given in Figure 3.5. If the initial input to the first stage is within $\pm 0.5V_{ref}$, all the stage output values will be within $\pm 0.5V_{ref}$ for an ideal converter. Since the basic idea of testing the converter is to apply the random signal of the last stage as an input to the first stage with a requirement that the random signal cover the entire converter input range, the output of the last stage is amplified by a gain of G such that the random input is approximately between $\pm V_{ref}$. Now if non-idealities are considered in

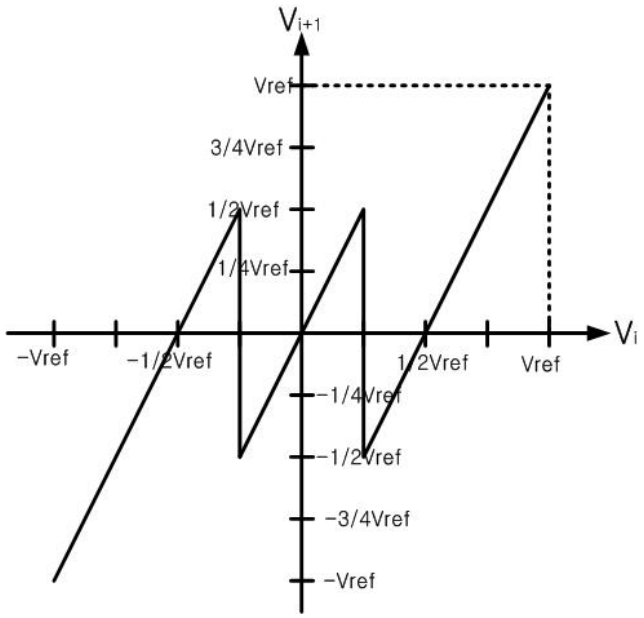


Figure 3.5: Ideal Transfer Characteristic for a 1.5 bit Stage

the converter, the last stage gain G must be selected such that no saturation

will happen in any of the stages. For a 1.5 bit pipeline stage with capacitor mismatch of α_i, amplifier offset of o_{ai}, comparator offset of o_{ci1} and o_{ci2}, the output of stage i given as V_{i+1} can be written as

$$V_{i+1} = (2 + \alpha_i)V_i - D_i(1 + \alpha_i)V_{ref} + o_{ai} \tag{3.7}$$

The transfer characteristic of stage i is illustrated in Figure 3.6. If the maximum variations on offset errors and mismatch error for all the stages are o_a, o_c and α, respectively, then the maximum absolute value of X in Figure 3.6 can be determined as

$$X = (2 + \alpha) \times (0.25V_{ref} + o_c) + o_a \tag{3.8}$$

When the last stage output is fed back to the first stage, the output of the first stage should be within $\pm V_{ref}$ to avoid saturation of the first stage. This can be achieved if G is selected using

$$G \leq \frac{(2 + \alpha)V_{ref} - o_a}{(2 + \alpha)X} \tag{3.9}$$

From the above equation, G must be chosen to be less than 2 to avoid saturation. Due to this requirement, the self-generated random signal at the converter input cannot cover the entire converter input range and hence, the measurement of the DNL and INL should be taken only within the valid sub-range that the pseudo random input covers. To determine the minimum valid range, the mismatch and offset errors for all stages are assumed to be equal to the maximum variation values. Then the random input $V_1(k)$ to the first

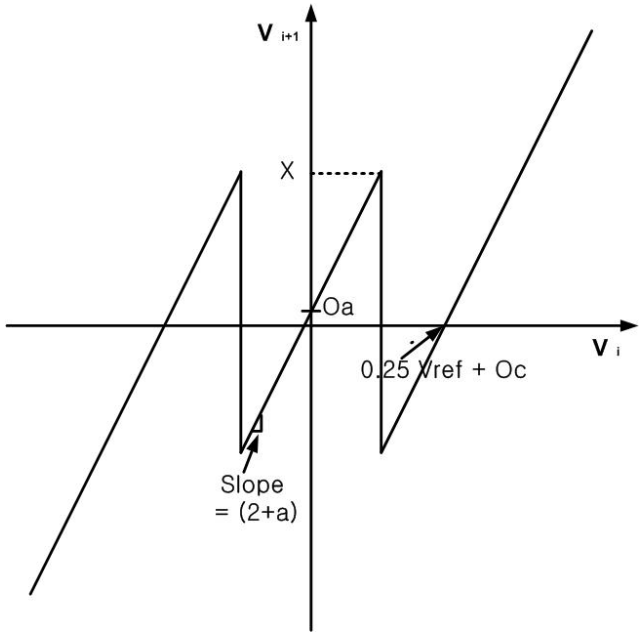


Figure 3.6: Transfer Characteristic with Mismatch and Offset Errors

stage at iteration k is assumed to be equal to the maximum valid input value for measurement and is just slightly less than V_{ref}. As a result, all the values of D_i from stage 1 to N are equal to -1. Then the output of the N stage $V_N(k)$ due to $V_1(k)$ can be determined to be

$$V_N(k) = (2+\alpha)^{N-1}V_1(k) - [(1+\alpha)V_{ref} - o_a]\sum_{j=o}^{N-2}(2+\alpha)^j \qquad (3.10)$$

If G is selected according to Equation (3.9), then $V_N(k)G \leq V_1(k)$. Using this equality and Equation (3.10), $V_1(k)$ and hence the minimum valid range R for measuring DNL and INL can be determined as

$$R = \frac{[(1+\alpha)V_{ref} - o_a]\sum_{j=o}^{N-2}(2+\alpha)^j}{G(2+\alpha)^{N-1} - 1} \tag{3.11}$$

In reality, the valid range is usually larger since the errors in most of the pipeline stages are less than the maximum tolerance values. Depending on the choice of transfer characteristic of the pipeline stage, the need for an extra gain G and the saturation problem can be avoided in random signal generation. As an illustration, the transfer characteristic shown in Figure 3.7 has a minimum valid range that is very close to the entire converter input range (i.e. $\pm V_{ref}$) by feeding the last stage back to the first stage directly without any additional amplification. If covering of the entire converter range is to be ensured, a gain of slightly higher than one can be used in the last stage. Notice that each stage will not suffer from saturation problems since the input to a stage must be higher than V_{ref} or lower than -V_{ref} by $0.5V_{ref}$ ideally for saturation to occur.

As mentioned at the beginning of this section, error in measuring DNL and INL using random inputs will be higher than the ramp input histogram test, due to higher uncertainty in the number of occurrences. To increase the confidence level in the measurement, more samples for constructing the histogram should be used. From the simulation results, the number of output samples and hence the value of H_{ideal} should be more than 20 times than those values for the case when the ramp input is used. This may not be attractive if the converter is tested with automated test equipment. However, for in-field

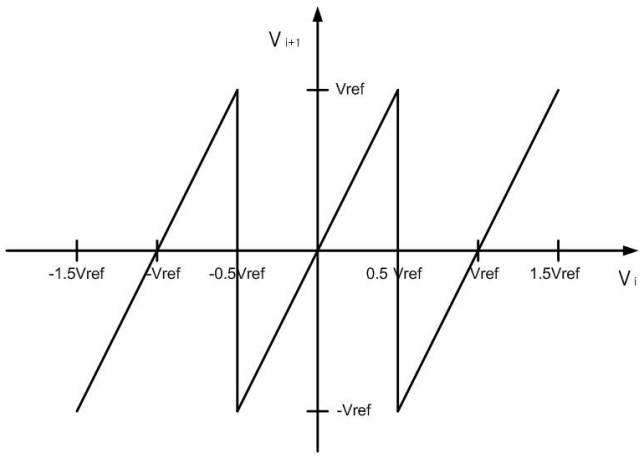


Figure 3.7: Transfer Characteristic with no Saturation Problem.

verification, this is usually acceptable in many applications. Besides, since no input signal is required in testing the converter, background self-testing is possible with the skip-and-fill background calibration technique [18]. When this calibration technique is used, one of the input samples is skipped every fixed number of clock cycles. During this cycle, the converter will perform calibration and the missing input sample is filled by digital interpolation using other samples. Although, after calibration, no input sample is actually needed to skip, the input can be skipped once in every N cycles for the purpose of measuring INL and DNL by connecting the input of the first stage to the output of the last stage every N cycles as illustrated in Table 3.2. If a longer time between skipped samples is required, the output of the last stage should be held until the next time that the feedback connection to the first stage is scheduled.

Table 3.2: Scheduling of Background Self-Testing Using the Skip-and-Fill Method.

Cycle	Phase	1	2	3	4	5	6
1	ϕ_1	S_{11}					
	ϕ_2		S_{12}				
2	ϕ_1	T		S_{13}			
	ϕ_2		T		S_{14}		
3	ϕ_1	S_{31}		T		S_{15}	
	ϕ_2		S_{32}		T		S_{16}
4	ϕ_1	S_{41}		S_{33}		T	
	ϕ_2		S_{42}		S_{34}		T
5	ϕ_1	T		S_{43}		S_{35}	
	ϕ_2		T		S_{44}		S_{36}
6	ϕ_1	S_{61}		T		S_{45}	
	ϕ_2		S_{62}		T		S_{45}
7	ϕ_1	S_{71}		S_{63}		T	
	ϕ_2		S_{72}		S_{64}		T
8	ϕ_1	T		S_{73}		S_{65}	
	ϕ_2		T		S_{74}		S_{66}
9	ϕ_1	S_{91}		T		S_{75}	
	ϕ_2		S_{92}		T		S_{76}
10	ϕ_1	S_{101}		S_{93}		T	
	ϕ_2		S_{102}		S_{94}		T
11	ϕ_1	T		S_{103}		S_{95}	
	ϕ_2		T		S_{104}		S_{96}
12	ϕ_1	S_{121}		T		S_{105}	
	ϕ_2		S_{122}		T		S_{106}
13	ϕ_1	S_{131}		S_{123}		T	
	ϕ_2		S_{132}		S_{124}		T

3.5 Behavior Simulation Result

The proposed technique was simulated using MATLAB. The pipeline ADC was assumed to have 12 bits of resolution. A 1.5 bit per stage that has the ideal transfer characteristic shown in Figure 3.5 was assumed. The total number of stages including the two redundant stages was 14. The mismatch error was assumed to be 5%. To illustrate the operation of background calibration, a ramp input signal was assumed at the input. This signal is not only used as the input signal in the simulation but is also used for measuring the

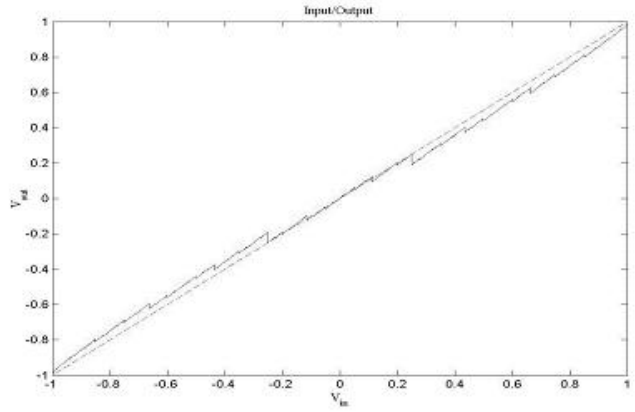
INL and DNL of the ADC.

3.5.1 Background Calibration

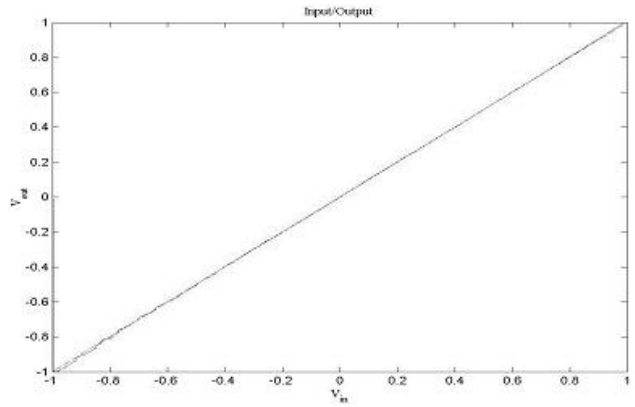
Figure 3.8 shows the output digital codes for the cases without and with background calibration. For the case without calibration, the DNL and INL plots are shown in Figure 3.9. The maximum DNL error and INL error are more than 10 LSBs. When background calibration was first applied, the ADC has a large non-linearity error at the beginning as indicated in Figure 3.10 and is the same as the non-calibrated case. However, the results get better after more calibration cycles. The DNL and INL plots are shown in Figure 3.10, which was measured when the calibration process was in progress. Therefore, the x-axis indicates both the digital code output and the time intervals. It can be observed that the DNL errors are almost zero as the time interval increases. However, the INL errors are non-zero for a large time interval due to the accumulated error at the beginning. If the ramp was applied again, the INL errors will also approach zero. Table 3.3 compares the results without calibration and with the proposed calibration technique.

Table 3.3: Comparison of INL and DNL Without Calibration and with Calibration.

Cycle	DNL Error	INL Error
Without Calibration	10 LSB	15 LSB
With Calibration	0.4 LSB	0.8 LSB

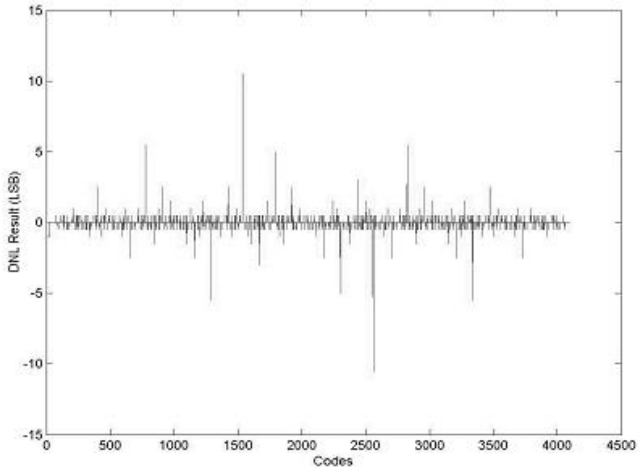


(a)

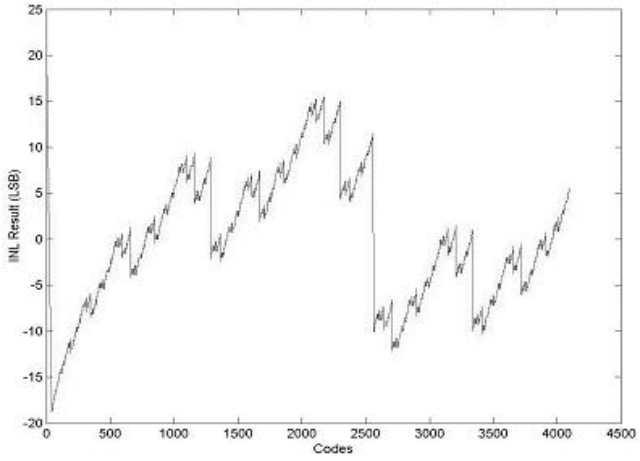


(b)

Figure 3.8: ADC Outputs for a Ramp Input: (a) Without Calibration and (b) with the Proposed Background Calibration.

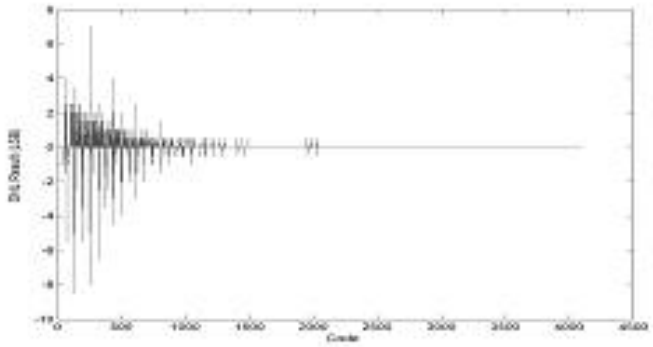


(a)

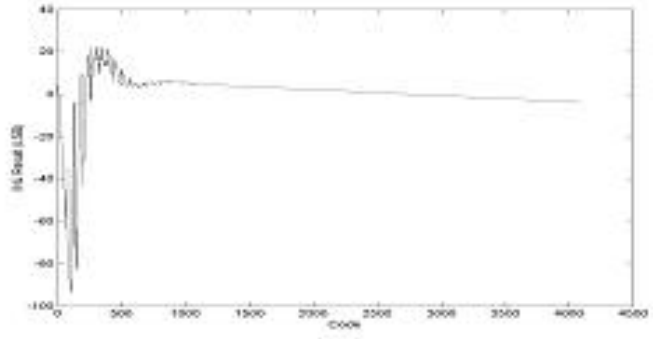


(b)

Figure 3.9: Non Linearity Test Without Calibration (a) DNL Result (b) INL Result.



(a)



(b)

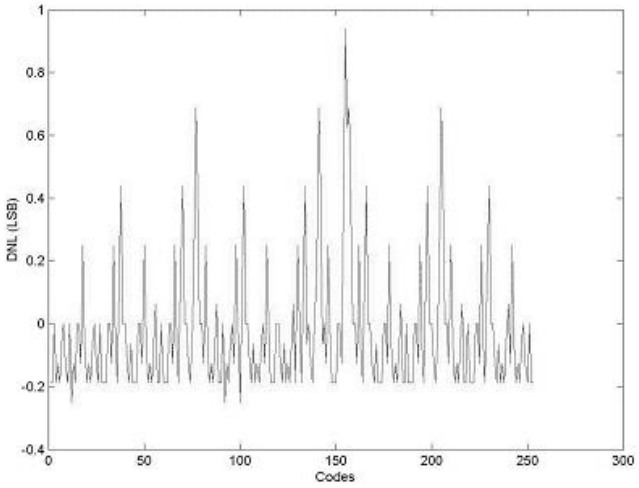
Figure 3.10: Non Linearity Test with Calibration (a) DNL Result (b) INL Result.

3.5.2 Histogram

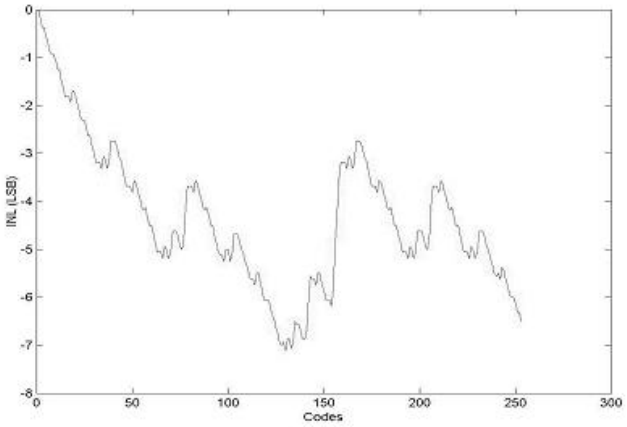
The background testing technique was also simulated based on MATLAB. In this case, in order to reduce the testing time, an 8 bit ADC was assumed. It also has a 1.5 bit per stage architecture. The DNL and INL plots with capacitor mismatch of 3% are shown in Figure 3.11 for a ramp input. In this case, H_{ideal} is equal to 16. To avoid saturation, G is selected to be 1.9 for the proposed technique. Using this selected G value, the valid range can be determined to be between $\pm 0.99\ V_{ref}$. From Equation (3.9), this range is very close to the entire converter's input range, so DNL and INL can be measured using this range. Figure 3.12 shows the DNL and INL results when H_{ideal} is equal to 128. The results shown on Figure 3.11 and Figure 3.12 are similar. The locations for large DNL errors are almost the same. The maximum differences in DNL and INL between the uses of a ramp input and the proposed technique are 0.4 LSBs and 1.3 LSBs, respectively. When H_{ideal} increases further, the difference becomes smaller. Hence, it can be concluded that both methods yield approximately the same results. Table 3.4 provides a comparison of the traditional ramp test and the proposed random input histogram test.

Table 3.4: Comparison of INL and DNL with a Ramp Input and with the Proposed Random Input Test.

Input	DNL Error	INL Error
Ramp	0.8 LSB	6.8 LSB
Random	1.1 LSB	7.1 LSB

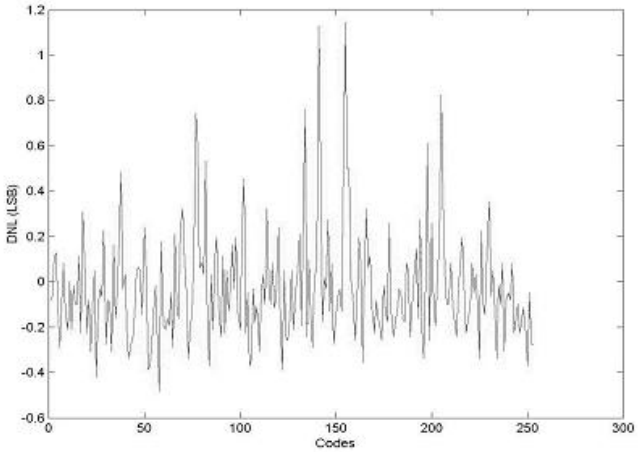


(a)

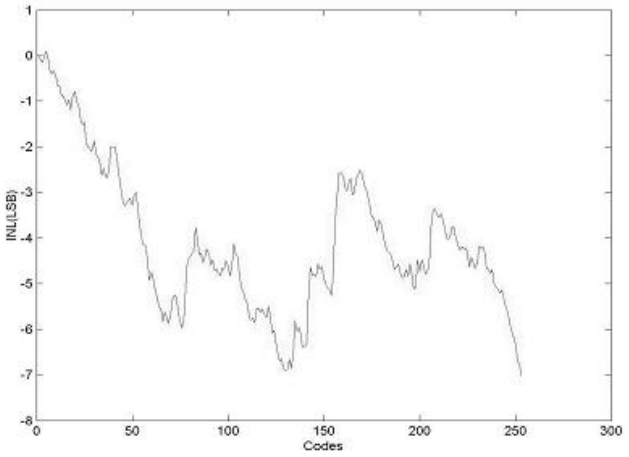


(b)

Figure 3.11: Non Linearity Test with a Ramp Input (a) DNL Result (b) INL Result.



(a)



(b)

Figure 3.12: Non Linearity Test with a Random Input (a) DNL Result (b) INL Result.

Chapter 4

Design of the Pipeline A/D Converter

In this chapter, basic circuits for the pipeline analog to digital converter such as switch blocks, sample/hold blocks and general techniques for the low-voltage switched-capacitor circuits such as boostrapping switches, comparators, and their advantages and disadvantages are described. A basic 1.5 bit/stage architecture (a very common block for the pipeline ADC) is also explained.

4.1 MOS Switches

In switched capacitor circuits, MOS switches are very commonly used. In [52][12], the errors attached to MOS switches are thoroughly handled. During the sample phase, the switch with an on-resistance r_{on} forms an RC circuit, the time constant of which defines the maximum signal bandwidth. A commonly used design rule for the time constant is that it should be at least five times larger than the settling time. However, the on-resistance r_{on} of an NMOS or PMOS switch is strongly dependent on the gate-source voltage V_{gs} of the transistor.

$$r_{on} = \frac{1}{\mu C_{ox}(\frac{W}{L})(V_{gs} - V_T)} \tag{4.1}$$

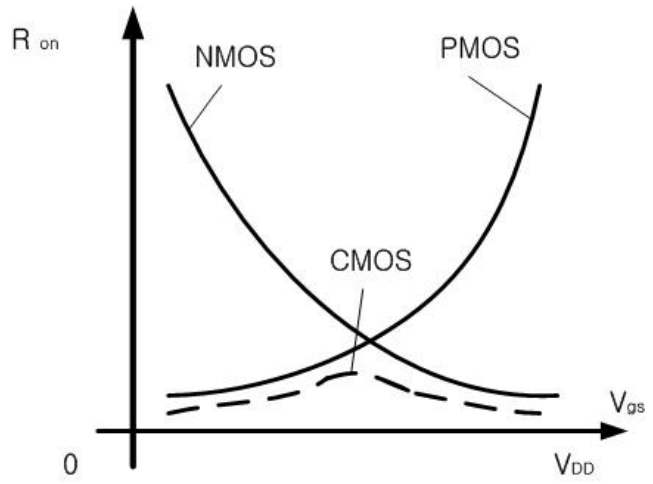


Figure 4.1: On Resistance of Different Types of MOS Switches.

Where: μ is the mobility, W and L are the width and length of the MOS transistor, respectively, C_{ox} is the gate oxide capacitance, and V_T the threshold voltage. Figure 4.1, shows the on-resistances of NMOS, PMOS, and CMOS switches plotted as a function of the gate-source voltage. This non-linearity of the switch on resistance generates distortion, which limits the allowable input signal swing. A CMOS switch consisting of parallel NMOS and PMOS transistors achieves a much higher linearity than the NMOS or PMOS alone. Nevertheless, it is still too high for high resolution ADCs. It is evident that the linearity of a MOS switch can be significantly improved if its gate-source voltage can be kept constant [34][53]. This can be accomplished by using the bootstrapping technique, described in the next Chapter.

4.1.1 Bootstrapped Input Switch

As the supply voltage of switched-capacitor circuit decreases, it becomes difficult to turn on the MOS switch. As shown in Figure 4.2, the NMOS transistor conducts for an input signal from 0 up to $V_{DD} - V_{tn}$ (threshold voltage of NMOS), and the PMOS transistor conducts for an input signal from $|Vtp|$ (threshold voltage of PMOS) to V_{DD}. The operation of the transmission gate fails when the supply voltage is less than $Vtn + |Vtp|$.

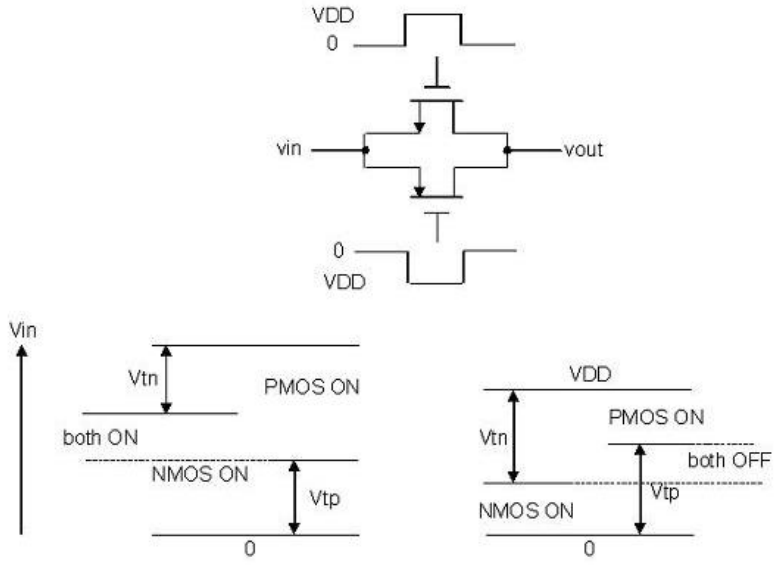


Figure 4.2: CMOS Transmission Gates with Different Gate Voltages.

There are several techniques to operate switched-capacitor circuits at a low supply voltage [54]. The first solution is reducing the threshold voltage of the transistors. This introduces more leakage current during off period of the switch, thus charge conservation cannot be applied accurately. The second

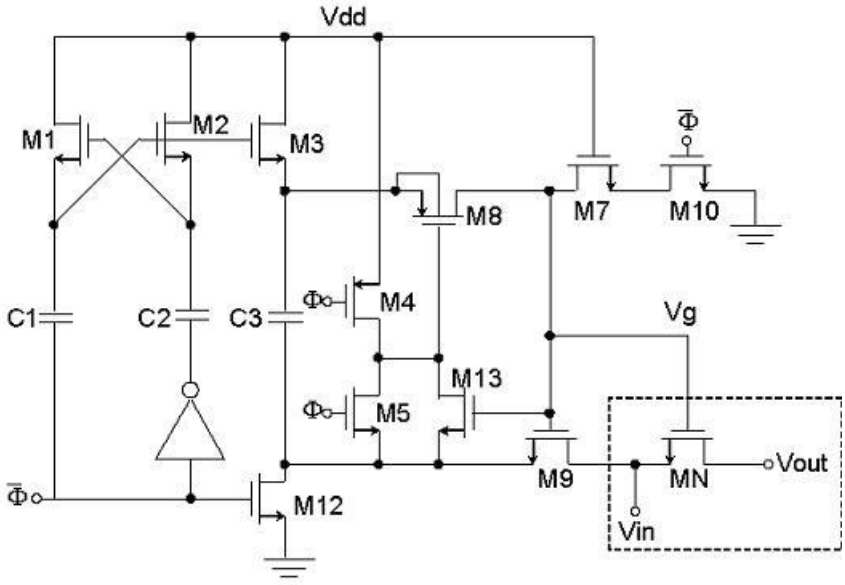


Figure 4.3: Boostrapping Circuit.

solution is increasing the gate voltage of the switch using either a charge-pump (voltage multiplier) circuit to generate a high supply voltage for the MOS switch or using a bootstrapping circuit for the gates of the switches. Both charge pump and bootstrap circuits require complex circuitry and may cause reliability problems. The bootstrapping circuit shown in Figure 4.3 [55][9][10].

Operation of the bootstrapped switch is as follows. When the switch is open, a capacitor C is precharged to V_{DD} and the switch transistor gate is short-circuited to ground, as shown in Figure 4.4(a). When the switch is closed in Figure 4.4(b), the transistor gate is disconnected from ground and the capacitor C is connected between the gate and source giving a signal independent gate overdrive of V_{DD}. As V_{gs} never exceeds the supply voltage,

reliability and brakedown voltage rules of the process are not violated. During the sample phase, when the switch is closed and the drain-source voltage V_{ds} is almost zero, a charge Q_{ch} is formed as

$$Q_{ch} = -WLC_{ox}(V_{gs} - V_t) \tag{4.2}$$

After the switch is opened by driving V_{gs} below V_T , the charge stored in the channel is distributed to the drain and source with a ratio depending on the impedance of these nodes and on the fall time of the driving gate signal. Since the injected charge is signal dependent through V_{gs}, the resulting error in the capacitor charging generates distortion [56][17].

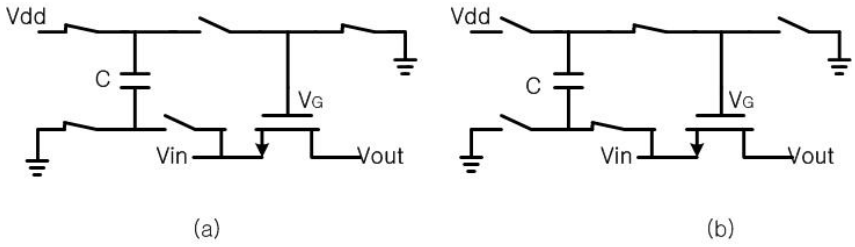


Figure 4.4: Principle of Boostintrapping (a) Switch Open and (b) Closed.

However, in reality, these constraints are never fulfilled and the cancellation is incomplete. In a bootstrapped switch as described above, the charge injection is always signal independent since the gate-source voltage is kept constant. Through the parasitic gate capacitances of a MOS switch the clock signal is connected to the signal propagating in the channel between the source and drain. Thus, the fast voltage gradients at the rising and falling clock edges cause an error in the charge sampled in a capacitor. The quantity of this clock

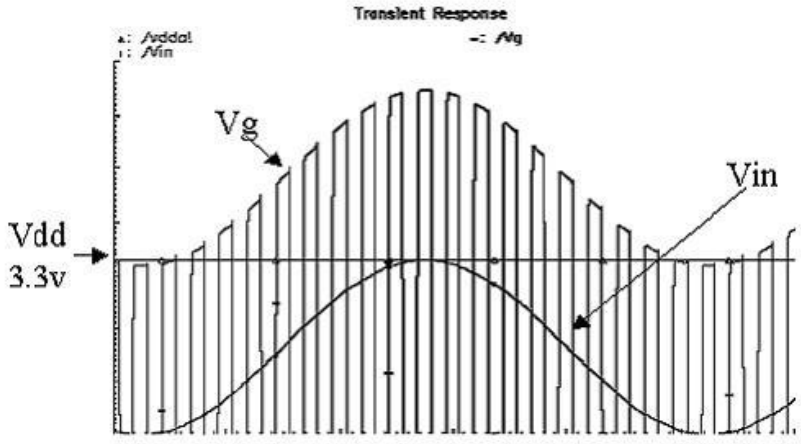


Figure 4.5: Input and Gate Voltage of Boostraping Circuit.

feedthrough error is proportional to the relation of the coupling and sampling capacitors and to the gradients of the clock signal [34]. As shown in Figure 4.5, the V_{gs} (gate-source voltage) of transistor is always constant regardless of the input voltage.

4.2 Sample-and-Hold (S/H)

The sample-and-hold is the most basic and ubiquitous switched-capacitor building block. Before a signal is processed by a discrete-time system, such as an ADC, it must be sampled and stored. This often greatly relaxes the bandwidth requirements of following circuitry which now can work with a DC

voltage. Because the S/H is often the first block in the signal processing chain, the accuracy and speed of entire application cannot exceed that of the S/H. In

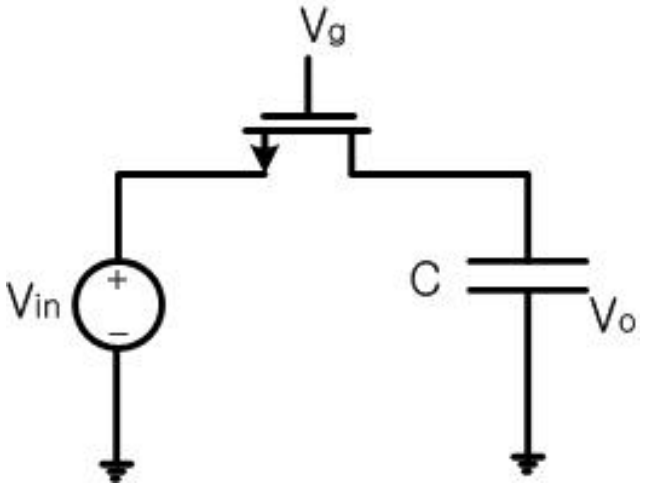


Figure 4.6: MOS Sample and Hold Circuit.

a CMOS technology, the simplest S/H consists of a MOS switch and a capacitor as shown in Figure 4.6. When V_g is high the NMOS transistor acts like a linear resistor, allowing the output V_o to track the input signal V_{in}. When V_g transitions low, the transistor cuts off isolating the input from the output, and the signal is held on the capacitor at V_o.

There are several practical limitations to this circuit. Because the RC network has finite bandwidth, the output cannot instantaneously track the input when the switch is enabled [8]. Therefore, a short acquisition period must be allocated for this (exponentially decaying) step response. After the S/H has acquired the signal, there will be a tracking error due to the non-zero phase lag and attenuation of the sampling network. The latter linear, low-pass filtering

does not introduce distortion and is usually benign for most applications. The on-conductance, however, of the transistor is signal dependent

$$g_{ds} = \mu C_{ox} \frac{W}{L}(V_g - V_T - V_i) \tag{4.3}$$

Thus the transfer function from input to output can become significantly non-linear if $V_g - V_i - V_t$ is not sufficiently large. A detailed analysis of these dynamic errors can be found in [57]. When the switch turns off, clock feed-through and charge injection introduce error in the output. When the gate signal V_g transitions from high to low, this step AC couples to the output V_o via parasitic capacitances, such as C_{gs} and C_{gd}.

4.2.1 Timing Skew Insensitive Double Sampled S/H Circuit

The main idea of the double sampling is to make utilization of the opamp more efficient, this is done by sharing the opamp with two parallel circuits, which is possible because of the opamp is needed only during one half of the clock cycle, but this technique sometimes creates a new problem. Because of the inherent parallelism of this technique, the circuit becomes susceptible to timing skew and is thus incapable of performing its main task. By modifying the standard double-sampled circuit, it can be made insensitive to the skew [58][59].

The main idea in this modification is to take away the parallelism from the sampling operation. This is accomplished by replacing the two parallel sampling switches with a single shared switch that is controlled with short

pulses at the full sampling rate. A simplified schematic of the circuit and its timing diagram are shown in Figure 4.7. Figure 4.8 is the simulation result of the circuit. The sampling to the upper capacitor is done by applying a short zero pulse to the switch S_0 during which the switches S_1 and S_3 are conducting. Consequently, the input voltage is sampled in capacitor C_{S_1} which is next connected into the feedback configuration around the opamp. After the sampling pulse the lower half circuit can begin its tracking phase, which will be concluded with a similar sampling event.

4.3 Comparator

The purpose of the comparator in an ADC is to compare the input voltage with a reference voltage. The simplest way is to apply input and reference voltage to a latch. Owing to the positive feedback characteristic of latch, the output signal is amplified to High or Low. The offset voltage of a latch is so large (as large as 100mV) that a pre-amplifier is usually added in the previous stage to enlarge the difference between input signal and reference voltage. There exists non-idealities for comparators, such as hysteresis and offset. Hysteresis is a memory effect causing decisions to be dependent on the previous state.

Figure 4.9 shows a comparator suitable for use in a two-phase, switched-capacitor circuit. For simplicity, a single-ended version is shown but this circuit can be extended to a fully differential implementation. During phase 1 the input signal V_{in} is sampled across capacitor C. Bottom plate sampling is

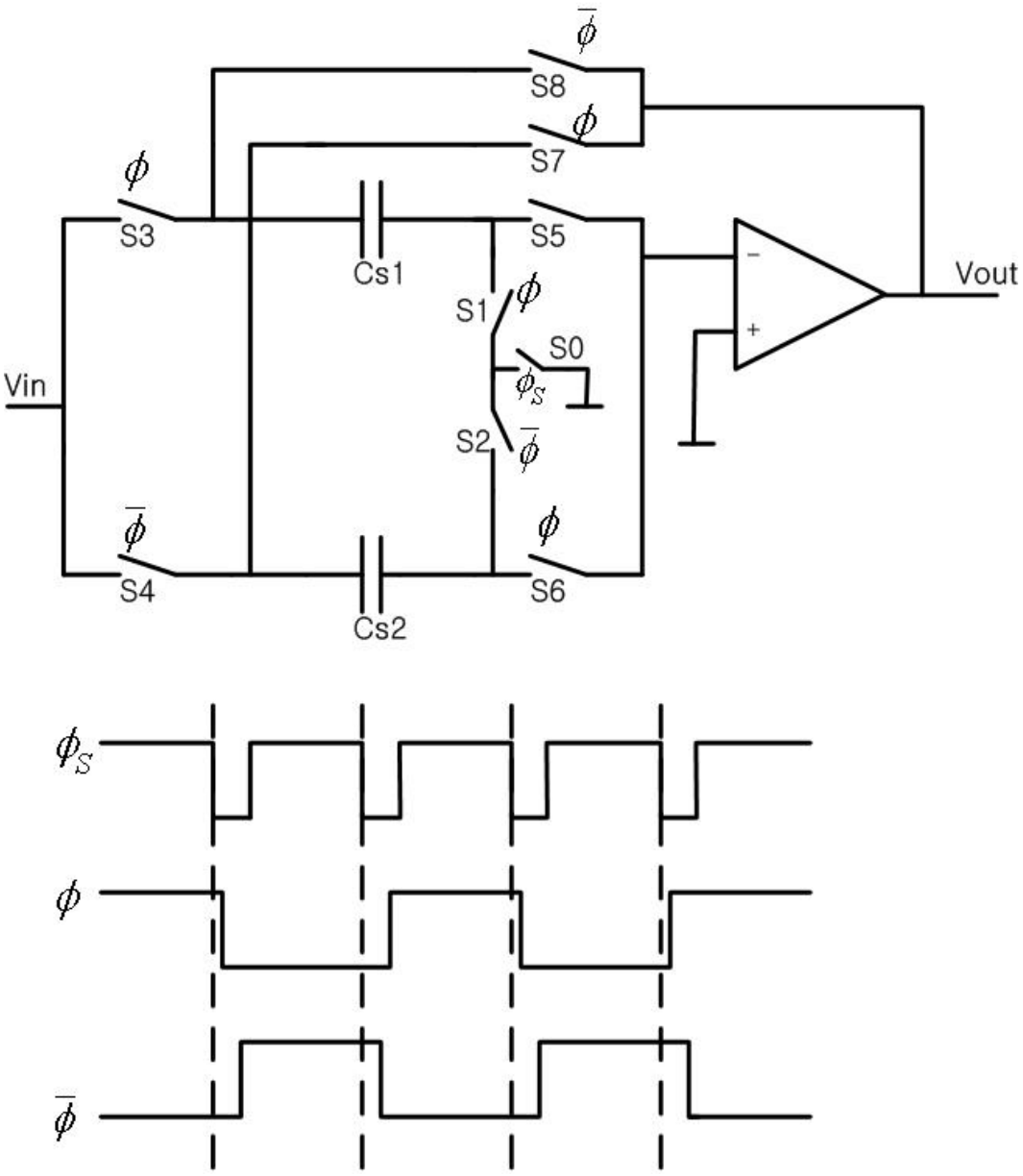


Figure 4.7: Skew Insensitive Double-Sampled S/H Circuit and its Timing.

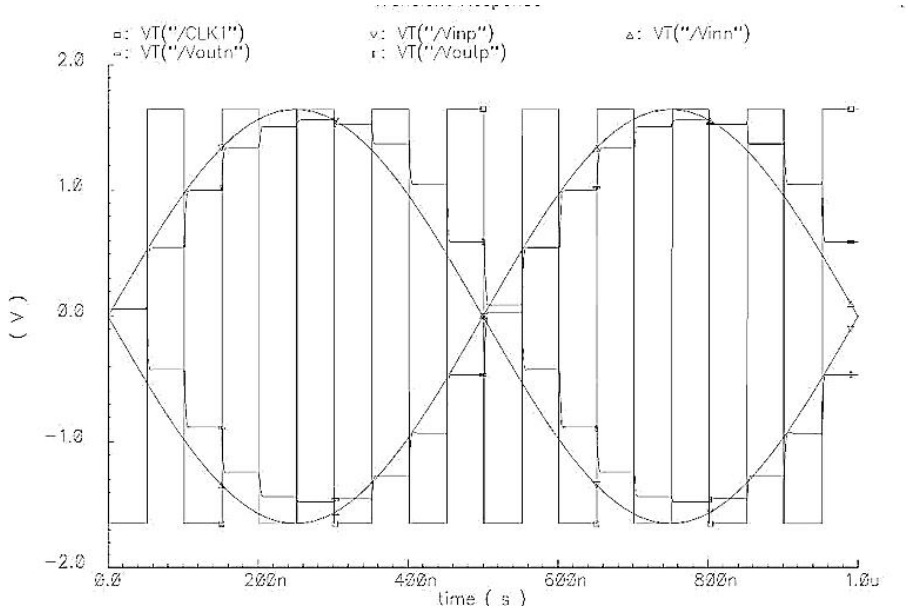


Figure 4.8: Skew Insensitive Double-Sampled S/H Circuit Simulation Result.

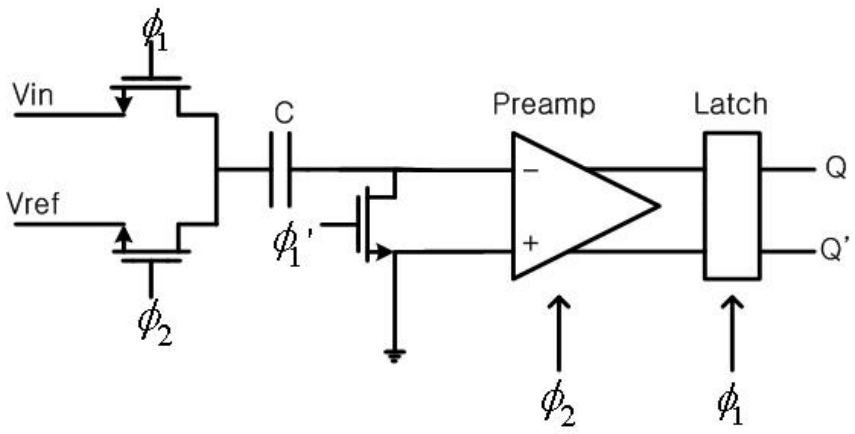


Figure 4.9: Schematic of the Comparator Block.

employed using the early clock phase ϕ_1' . During phase 2 the reference voltage V_{ref} is applied to the left side of the capacitor. The voltage difference

$(V_{ref} - V_i)$ appears at the input of the pre-amplifier. The pre-amplifier amplifies this difference and applies it to the input of a regenerative latch. At the end of phase 2 the pre-amplifier outputs are disconnected from the input. At the beginning of phase 1 of the next cycle, the latch is strobed, creating digital logic levels at the output.

Any offset voltage of the pre-amplifier is directly referred to the input of the comparator. The potentially large offset of the latch is divided by the small-signal gain of the pre-amplifier when referred to the input. Multiple pre-amplifiers can be cascaded to further reduce the effective latch offset at the expense of power consumption. If a low offset is required, auto-zero techniques can be employed in the pre-amplifier [60][30].

4.4 Clock Generator

In this pipelined ADC, the required clock phases are CLK1, CLK1-bar, CLK2, CLK2-bar, CLK1a, CLK1a-bar, CLK2a, CLK2a-bar, CLK1 and CLK2 are non-overlapping clocks and CLK1a and CLK2a are slightly delayed from CLK1 and CLK2 in order to reduce charge injection and clock feedthrough effects.

As shown in Figure 4.10, CLK1 and CLK2 are generated by a non-overlapping clock generator. Adjusting the W/L ratio of inverters can properly adjust the non-overlap period. CLK1a and CLK2a are generated by adding several inverters behind CLK1 and CLK2. The outputs of inverters, such as CLK1 and CLK2, are frequently used. The W/L ratio of these inverters can

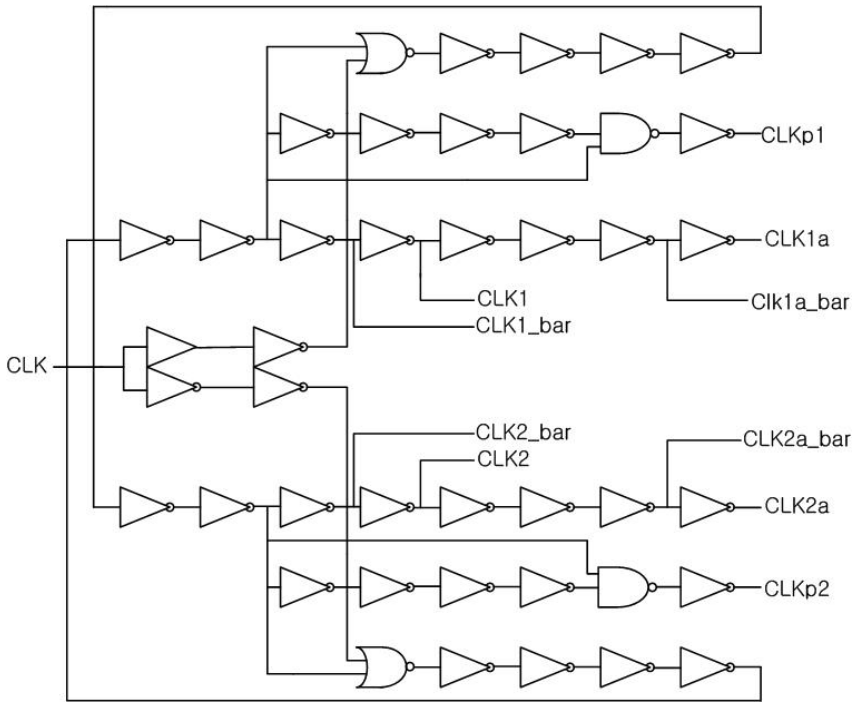


Figure 4.10: Schematic of the Clock Generation Block.

be adjusted to improve the driving ability.

4.5 1.5 bit/Stage Architecture

This architecture operates with non-overlapping clocks, ϕ_1 and ϕ_2, ϕ_{1d} is the delayed version of ϕ_1. When ϕ_1 (ϕ_{id}) is high, the input is sampled on C_s and C_f capacitors. At the same time, sub-ADC compares the input with two reference voltages ($V_{ref}/4$ and $-V_{ref}/4$), and produces a stage output code which will be collected and corrected by the digital correction circuit.

From Equation (4.7), the total charge is $2CV_{in}$ at the end of the ϕ_1

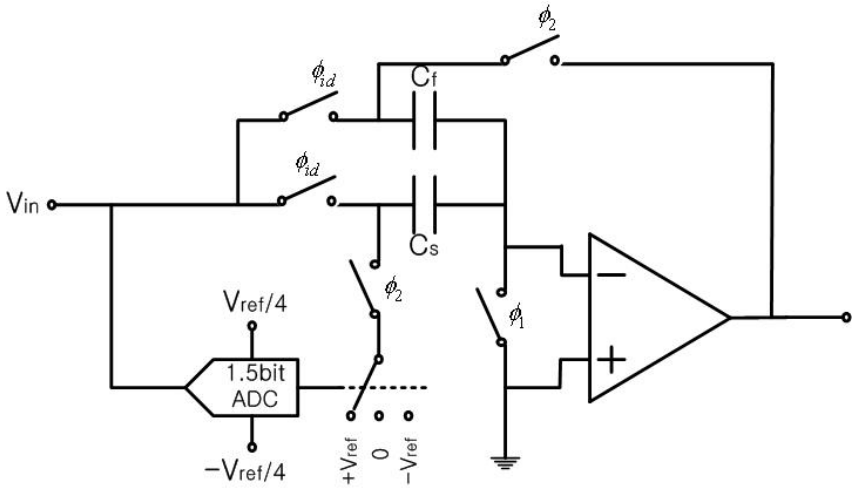


Figure 4.11: 1.5 bit Pipeline Stage Architecture.

phase.

$$Q_f = C_f(V_{in} - 0), \tag{4.4}$$

$$Q_s = C_s(V_{in} - 0) Q_{\phi_1} = Q_f + Q_s = (C_f + C_s)V_{in} \tag{4.5}$$

$$\text{Since} \quad C_f = C_s = C Q_{\phi_1} = 2CV_{in} \tag{4.6}$$

$$Q_{\phi_1} = 2CV_{in} \tag{4.7}$$

When ϕ_2 is high, the capacitor C_s is connected to $\pm V_{ref}$ or 0 according to sub-ADC output code, and capacitor C_f forms the feedback loop.

From Equation (4.12), the total charge at the end of ϕ_2 phase is $C(V_{out} \pm V_{ref}) - 2CV_{offset}$.

$$Q_f = C_f(V_{out} - V_{offset}), \tag{4.8}$$

$$Q_s = C_s(V_{ref} - V_{offset}) \tag{4.9}$$

$$Q_{\phi_2} = Q_f + Q_s = C_f V_{out} + V_{ref} - (C_f + C_s)V_{offset} \tag{4.10}$$

$$Since \quad C_f = C_s = C \tag{4.11}$$

$$Q_{\phi_2} = C(V_{out} - V_{ref}) - 2CV_{offset} \tag{4.12}$$

Figure 4.12 is the simulation result of the 1.5 bit/stage architecture.

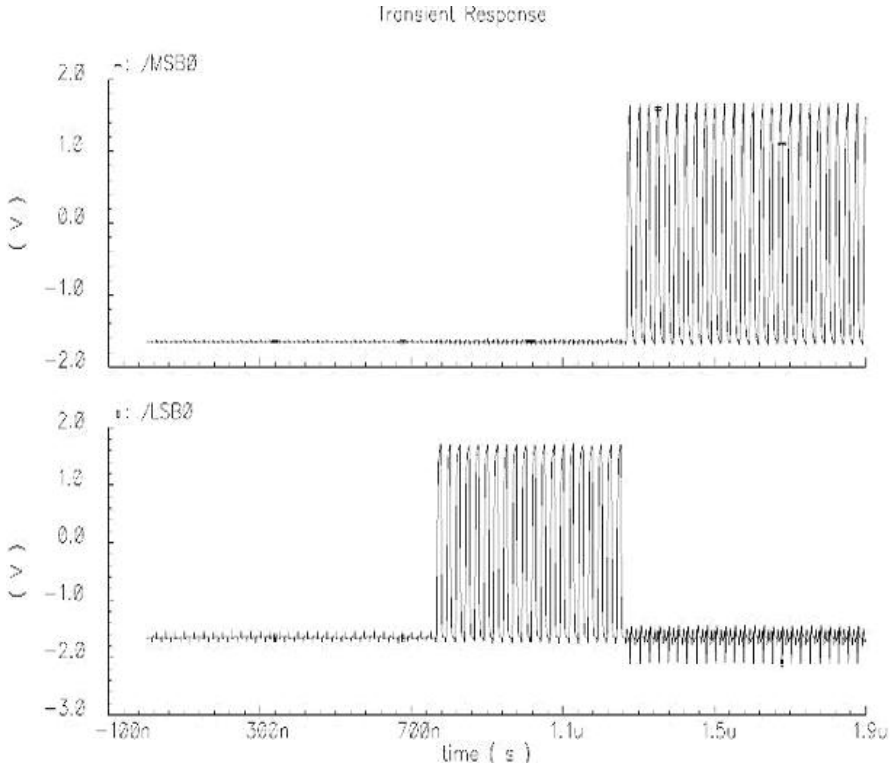


Figure 4.12: 1.5 bit Pipeline Stage Result.

4.6 Sub-DAC Circuit

The Sub-DAC Circuit is another key component used in each stage. The main role of a sub-DAC circuit is to supply the gainstage with an analog voltage level that represents the quantized portion of the input sample, This quantized portion is subtracted from the original signal to create the residue voltage [19]. In this design, the sub-DAC not only provides the analog output but also calculates the digital word sent to the digital correction logic circuit. Each stage can generate digital output 00, 01 or 10 for a digital word and the corresponding sub-DAC outputs will be $-V_{ref}$, 0 or $+V_{ref}$. Theoretically the locations are at $-V_{ref}/2$, 0 and $+V_{ref}/2$ but the sub-DAC outputs need to be multiplied by a gain of 2 in the gainstage after the sample/sub-DAC residue is generated. This gain of two is needed to ensure the sample remains in the proper threshold range as residue propagates from one stage to the next. In order to make the circuits simpler, the input sample and the sub-DAC outputs are multiplied by a factor of 2 before the sub-DAC output is subtracted to obtain the residue. The circuit for the sub-DAC was adapted from [55]. Figure 4.13 shows the combination of logic and switches needed to provide the outputs. The 3 NAND gates combine the clock signal and inputs from the differential comparators A1, A2, B1 and B2. A and B are outputs of the two differential comparators. The relationships between the outputs of the comparators are $A2 = \bar{A}1$ and $B2 = \bar{B}1$. Vdac1 and Vdac2 are the analog outputs connected to the gainstage. From the schematic shown on Figure 4.13, it can be seen that the output will only be valid when CLK2 is valid. Table

5.1 lists all the possible states of the sub-DAC.

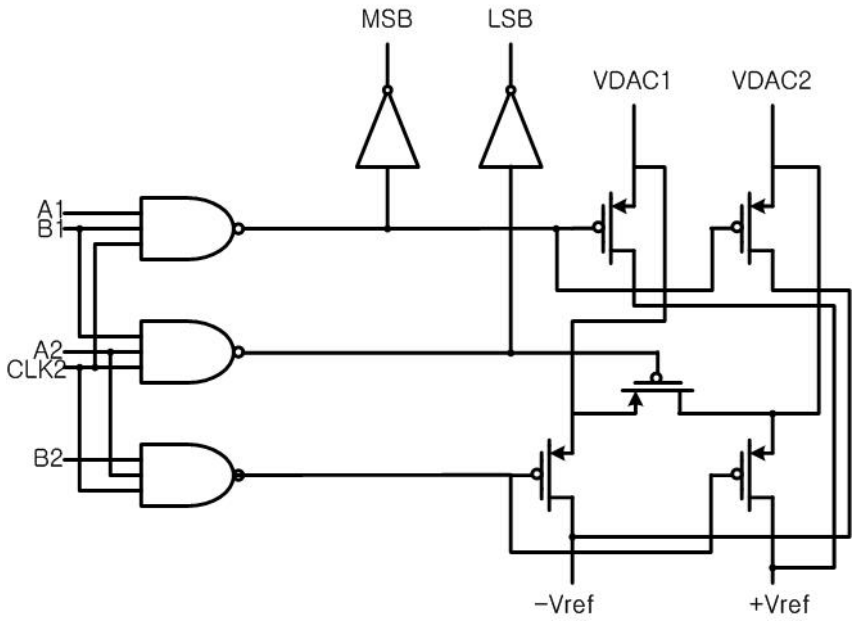


Figure 4.13: Schematic of Sub-DAC Block.

Table 4.1: Sub-DAC Output.

A1	A2	B1	B2	CLK2	MSB	LSB	V_{dac1}	V_{dac2}
0	1	0	1	1	0	0	$-V_{ref}$	$+V_{ref}$
0	1	1	0	1	0	1	V_{dac2}	V_{dac1}
1	0	1	0	1	1	0	$+V_{ref}$	$-V_{ref}$

Chapter 5

Design of the Operational Amplifier

The operational amplifier is the most critical block of a pipeline stage. The resolution and speed of the ADC is usually determined by the operational amplifiers. In general, the amplifier's open loop DC-gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximum clock frequency. To maximize the signal-to-noise ratio, the operational amplifier should also utilize a large signal swing at the output. The amplifier specifications vary relative to the resolution and sample rate of ADCs.

To get a very large open loop DC-gain for a high-resolution high-speed pipeline ADC, a wide bandwidth and a high slew rate are required from the amplifier [23][24]. The simplest way to meet these requirements is to use one-stage amplifiers, like the folded and telescopic cascode amplifiers, with gain boosting. The drawback of these topologies, especially with low supply voltage, is a limited signal swing and a complicated settling behavior because of the regulation amplifiers. High open loop DC-gain can also be achieved with a two or more stage amplifier. In multi stage amplifiers, a trade off in the frequency compensation exists between the stability and bandwidth. The operational

amplifier topologies and their design have been examined in [13][15].

The proposed two-stage high gain opamp is shown in Figure 5.1

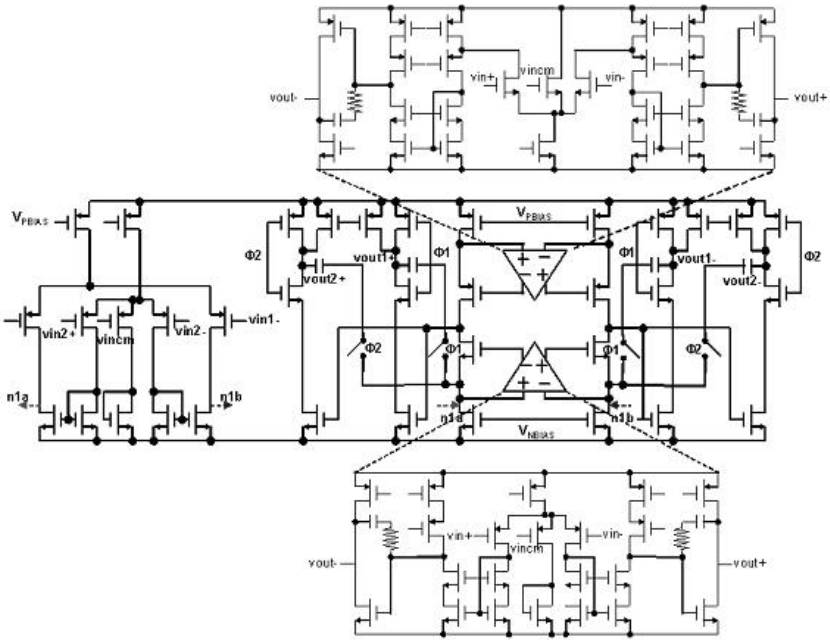


Figure 5.1: Two Stage High Gain Opamp.

Basically, this is a modified two-stage folded-cascode opamp [43]. There is one more transistor in the input stage, and this transistor takes care of the common-mode feedback. A large output signal swing is achieved by adding a second stage to the main amplifier. The gain-boosting amplifiers are used for both PMOS and NMOS cascode transistors. Figures 5.2 and 5.3 are the DC response and the AC response of the opamp, respectively. Table 5.1 summarizes the simulation results. A DC gain of 134.5 dB, a 219MHz gain bandwidth at a gain of 3 and a 60 degree phase margin were achieved with a 1.6V supply

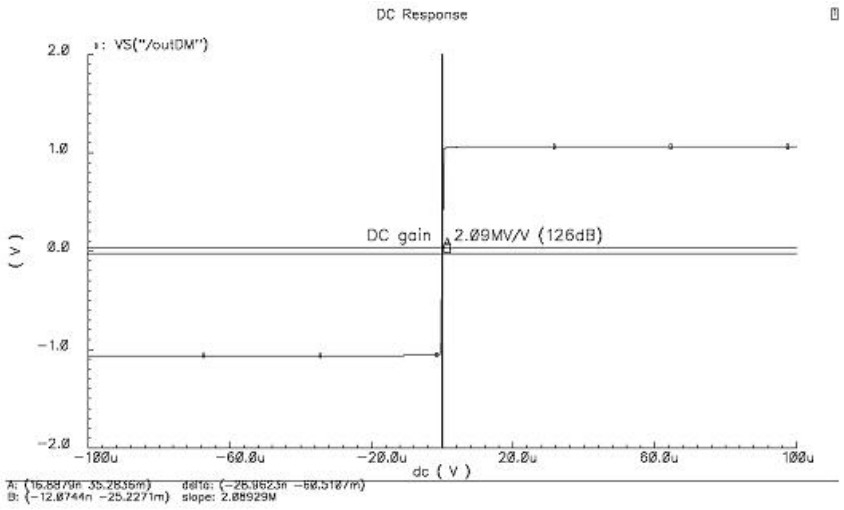


Figure 5.2: DC Response of the Two Stage High Gain Opamp.

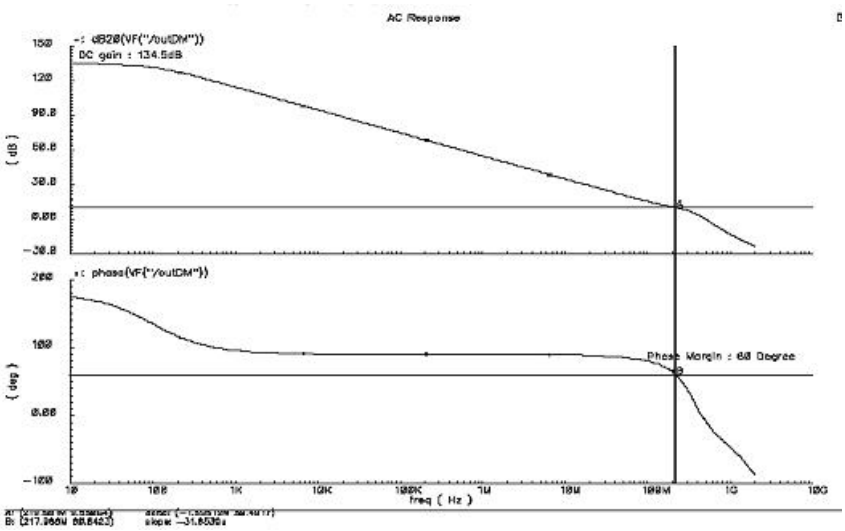


Figure 5.3: AC Response of the Two Stage High Gain Opamp.

voltage and 1.5pF load.

Table 5.1: Simulation Results.

Supply Voltage	1.6V
DC Voltage Gain	134.5dB
Gain Bandwidth	219Mhz
Phase Margin	60
Power Consumption	5.6mW

5.1 Main Amplifier Design

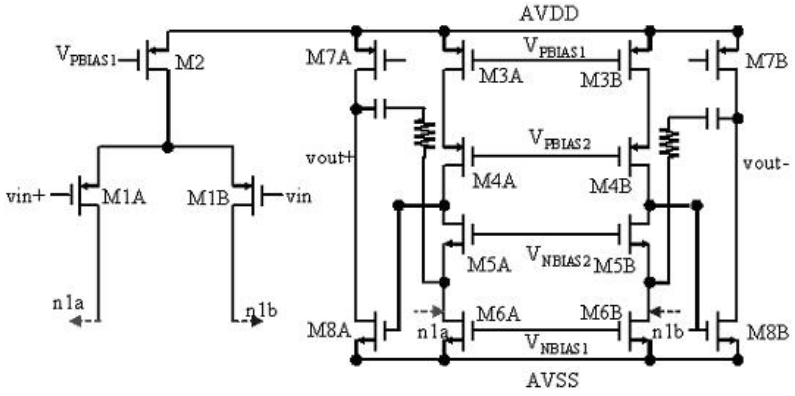


Figure 5.4: Simplified Schematic of the Main Amplifier.

Figure 5.4 shows the simplified schematic of the main amplifier. This is a two-stage folded-cascode amplifier with Ahuja-style compensation [65]. The reason for employing Ahuja-style compensation is that the compensation resistors are replaced by NMOS switches in the real amplifier, because this amplifier will be a switched-opamp, and the switches can be turned off to avoid discharging the compensation capacitors when the output of amplifier is connected to V_{DD} (the positive supply) or V_{SS} (the negative supply) [65].

However, it is difficult to turn on the switches if Miller compensation is used, because the Vgs (gate-source voltage) of the NMOS transistor is only 0.8V. Due to the body effect, 0.8V is not enough to turn on the switches. Table 5.2 shows the size of main amplifier and Figures 5.5 and 5.6 are DC and AC responses of the main amplifier

Table 5.2: Transistor Size of the Main Amplifier.

Transistor	Size m(W/L)	Transistor	Size m(W/L)
M1a(B)	8(6/0.4)	M5a(B)	8(6/0.6)
M2a(B)	20(6/0.4)	M6a(B)	8(6/0.6)
M3a(B)	12(6/0.4)	M7a(B)	56(6/0.6)
M4a(B)	10(6/0.4)	M8a(B)	20(6/0.6)

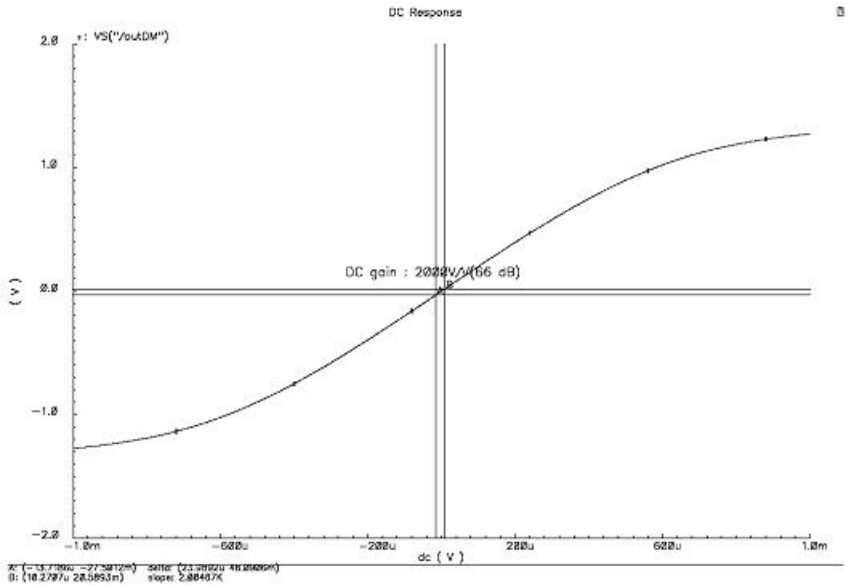


Figure 5.5: DC Response of the Main Amplifier.

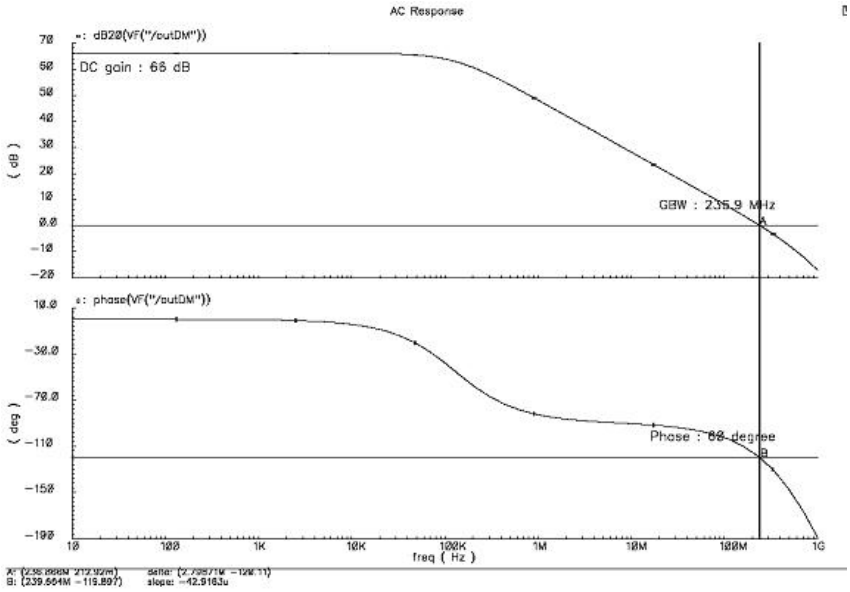


Figure 5.6: AC Response of the Main Amplifier.

5.2 PMOS Gain Boosting Amplifier

Figure 5.7 shows the gain-boosting amplifier for the PMOS cascode transistors. This is also a two-stage folded-cascode amplifier with Miller compensation. Even though the outputs of the main amplifier are connected to V_{DD} or V_{SS}, this amplifier keeps working, thus the compensation resistors don't need to be replaced by NMOS switches and the Miller compensation technique can be applied to this amplifier [11][12]. Since the output common-mode voltage is the bias voltage of PMOS cascode transistors and this is operating at a low supply voltage, the second stage (output stage) is utilized for providing the proper bias voltage for the PMOS cascode transistors. The common-mode feedback problem is solved by an additional input transistor and the feedback

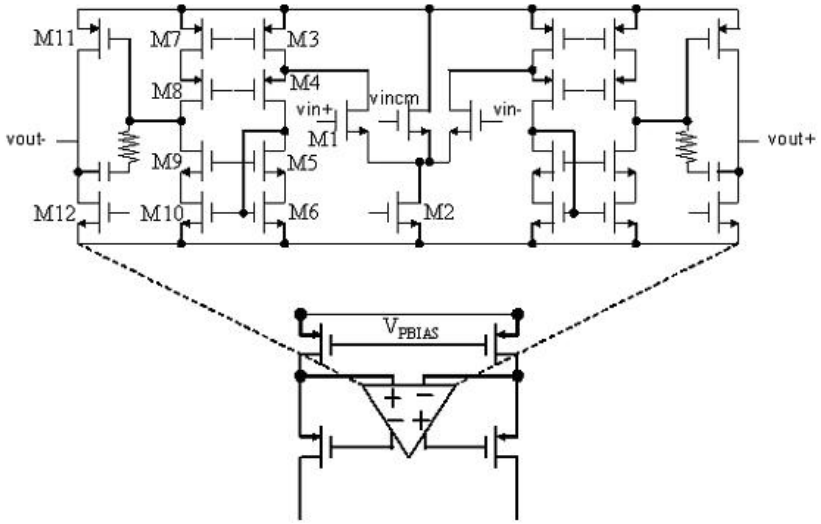


Figure 5.7: Schematic of the PMOS Gain Boosting Amplifier.

loop is formed by adding a signal path between the input stage and the output stage. The transistor sizes for the PMOS gain boosting amplifier are shown on Table 5.3. The DC and AC response of this circuit is shown on Figures 5.8 and 5.9, respectively.

Table 5.3: Transistor Size of the PMOS Gain Boosting Amplifier.

Transistor	Size m(W/L)	Transistor	Size m(W/L)
M1	4(2.4/0.6)	M7	2(6/0.6)
M2	4(2.4/0.6)	M8	2(6/0.4)
M3	4(6/0.6)	M9	2(3.6/0.4)
M4	2(6/0.4)	M10	2(3.6/0.4)
M5	23(3.6/0.4)	M11	8(4.8/0.4)
M6	2(3.6/0.4)	M12	4(2.4/0.4)

Basically, this amplifier does not need a complicated common-mode

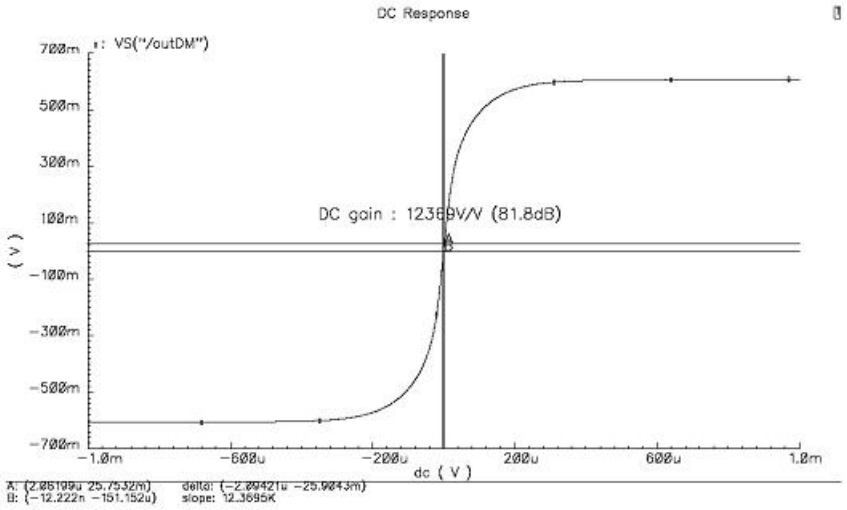


Figure 5.8: DC Response of the PMOS Gain Boosting Amplifier.

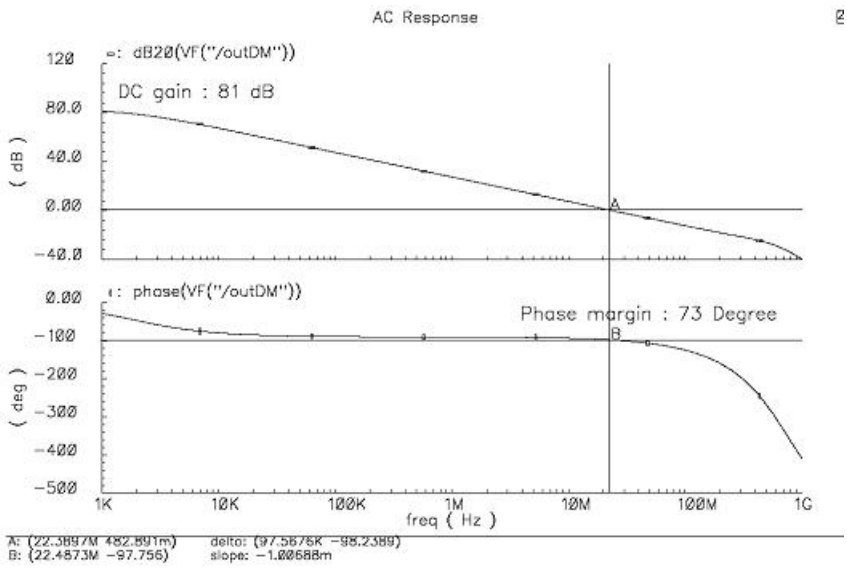


Figure 5.9: AC Response of the PMOS Gain Boosting Amplifier.

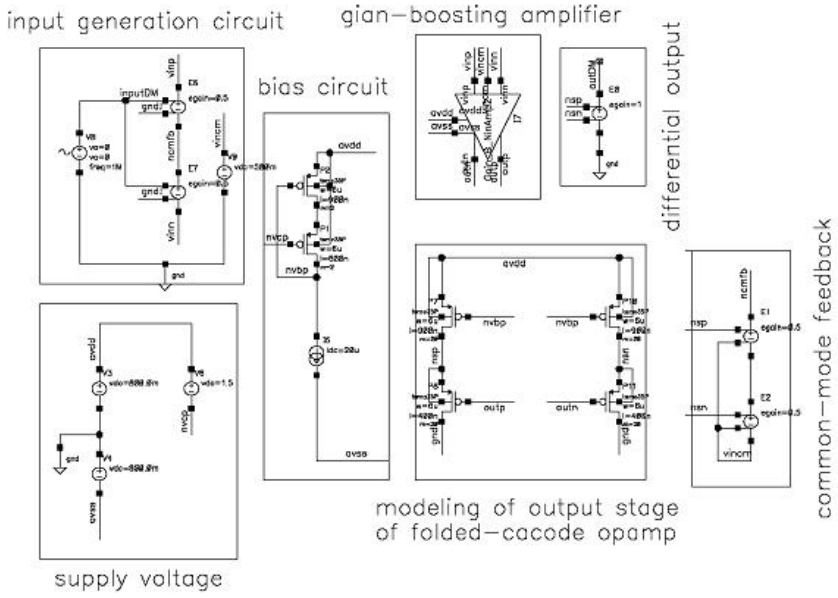


Figure 5.10: Test Circuit of the PMOS Gain Boosting Amplifier.

feedback (CMFB) circuit. Instead of using a conventional CMFB circuit, one transistor acts as a CMFB circuit, and this is possible only when input and output are tied together. Therefore, this special situation should be modeled when testing the circuit. Figure 5.10 shows the test circuit of this opamp. Input and output of the gain boosting amplifier are connected through the PMOS cascode transistors, and a voltage-controlled voltage-source is used as a CMFB circuit. An 81dB DC gain and a 73 degree phase margin are achieved by this amplifier.

5.3 NMOS Gain Boosting Amplifier

An NMOS gain boosting amplifier is shown on Figure 5.11. The basic structure is almost same as the one for the PMOS gain boosting amplifier except the input stage. The transistor sizes are given by Table 5.4.

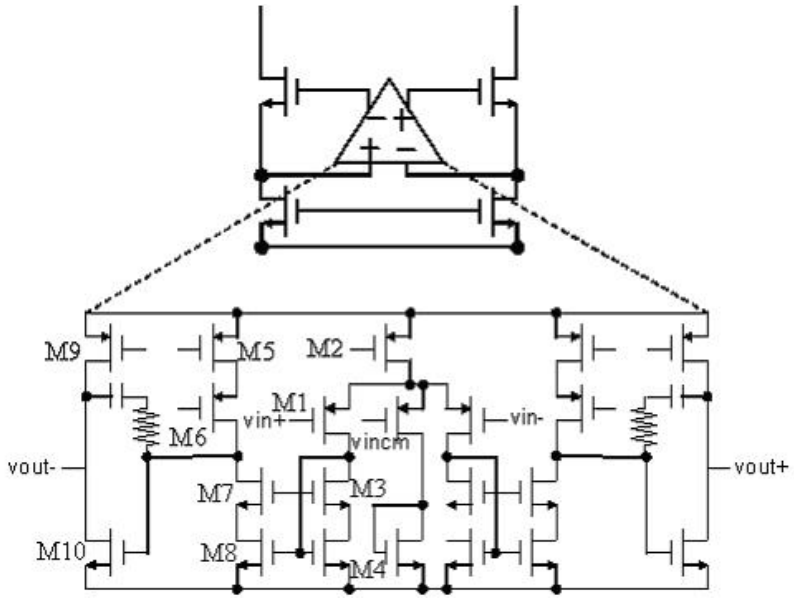


Figure 5.11: Schematic of the NMOS Gain Boosting Amplifier.

Table 5.4: Transistor Size of the NMOS Gain Boosting Amplifier.

Transistor	Size m(W/L)	Transistor	Size m(W/L)
M1	6(6/0.9)	M6	2(6/0.6)
M2	6(6/0.6)	M7	2(3.6/0.4)
M3	2(3.6/0.6)	M8	2(3.6/0.4)
M4	2(3.6/0.4)	M9	8(6/0.6)
M5	3(6/0.8)	M10	2(6/0.8)

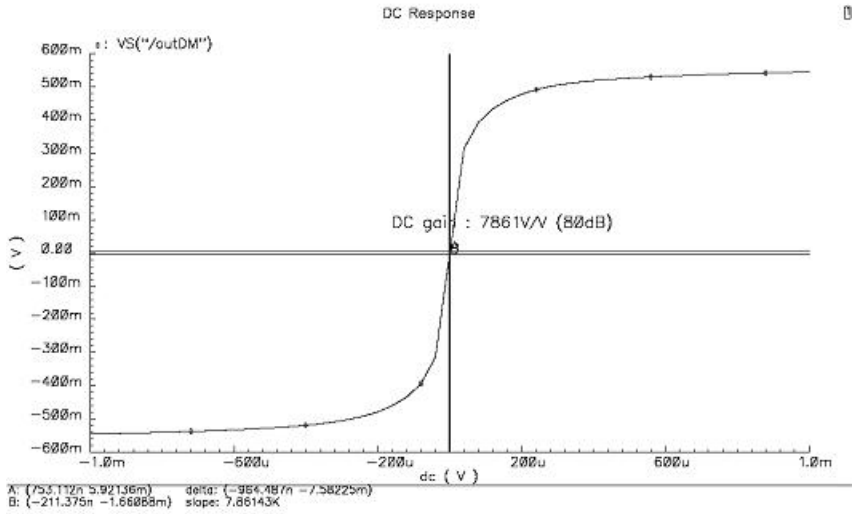


Figure 5.12: DC Response of the NMOS Gain Boosting Amplifier.

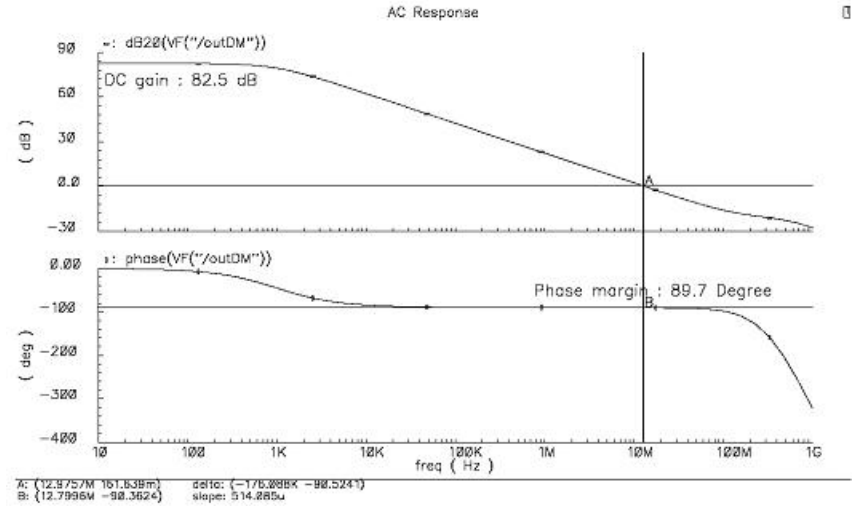


Figure 5.13: AC Response of the NMOS Gain Boosting Amplifier.

Figures 5.12 and 5.13 indicate that an 82.5dB DC gain and an 89.7 degree phase margin are achieved.

5.4 Gain Stage

Figure 5.14 shows a gain stage that samples the input, applies gain, and holds the output value. A single-ended version is shown for simplicity, but the following analysis applies to a differential version which is most commonly used in practice. To better understand the operation of this circuit, Figures

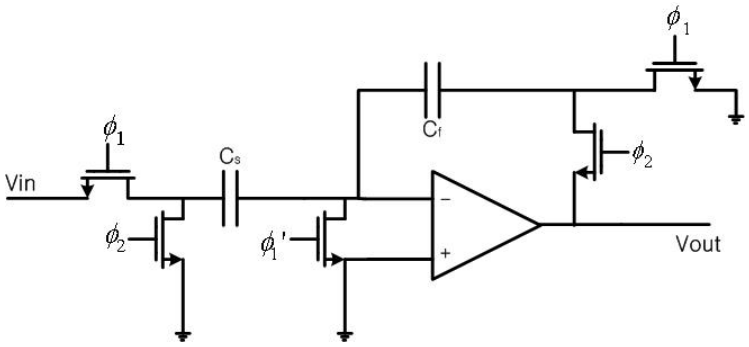


Figure 5.14: Schematic of Single End Gain Stage.

5.15a and 5.15b show the states of the switches during phase 1 and phase 2 respectively. During phase 1 (Figure 5.15a), the input V_i is sampled across C_s. The opamp is not used during this phase, and this time can be used to perform auxiliary tasks such as resetting common-mode feedback. The charge Q_{ch} is:

$$Q_{ch} = C_s(0 - V_i) = -C_s V_i \tag{5.1}$$

Notice there is no charge stored on C_f since both sides are grounded. Bottom-plate sampling is employed, and the sampling instant is defined as before. During phase 2 (Figure 5.15b), the opamp is put in a negative feedback

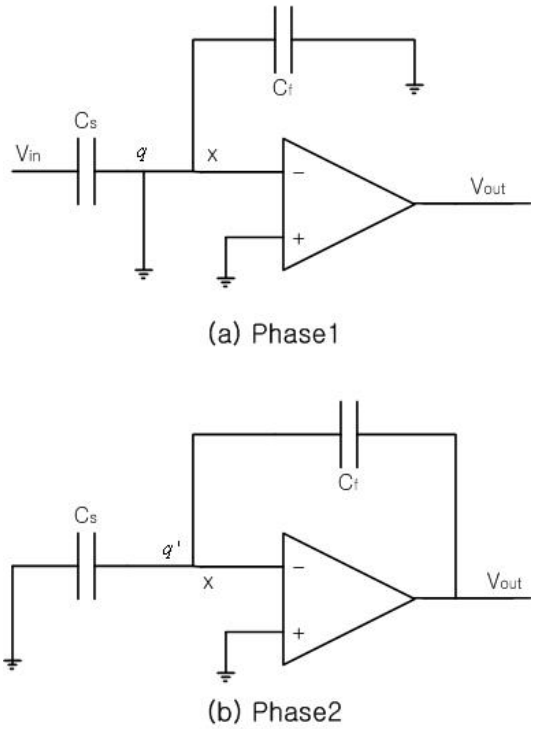


Figure 5.15: Gain Stage.

configuration, forcing node X to zero (virtual ground). Because the input is also ground, there is no charge storage on Cs, and all the charge is transferred to C_f . Thus, a voltage gain of C_s/C_f is achieved. Analytically, the charge on node X is conserved, So using the equation $q = q'$, a voltage gain is expressed as

$$-C_s V_i = C_f(0 - V_o) \tag{5.2}$$

$$\frac{V_o}{V_i} = \frac{C_s}{C_f} \tag{5.3}$$

If the input V_i is considered as a discrete-time sequence $V_i(n) = V_i(nT)$, where T is the sampling period, then the output is expressed as

$$V_o(n) = \frac{C_s}{C_f} V_i(n-1) \tag{5.4}$$

This equation reflects the one period latency of this circuit. Because this circuit incorporates an opamp, it has the same limitations as the sample-and-hold circuit. In addition, the exact gain of the stage is dependent on the matching of C_s and C_f . For example if $C_s = C_f + \Delta C$ then:

$$V_o(n) = \frac{C_s}{C_f} V_i(n-1) + \frac{\Delta C}{C_f} V_i(n-1) \tag{5.5}$$

In high-resolution applications, the second term can represent a significant error. Similarly if the capacitors have a voltage-dependent value, the gain will be distorted. Figure 5.16 shows the simulation results of the gain stage.

5.5 Verification of Scheduled Calibration Block

This section discusses the digital block for scheduling the calibration and testing cycles. The scheduling scheme was implemented using Verilog HDL and simulated using the Verilog-XL simulator. The Verilog-XL simulator is part of the Cadence software package. Figures 5.17-20 show the Verilog simulation results depending on the mode of the pipeline ADC. During the calibration mode, the select signal chooses the DAC value in order to convert it to a digital output. In the normal mode, the select signal chooses the previous stage residue output. In the testing mode the last stage output is

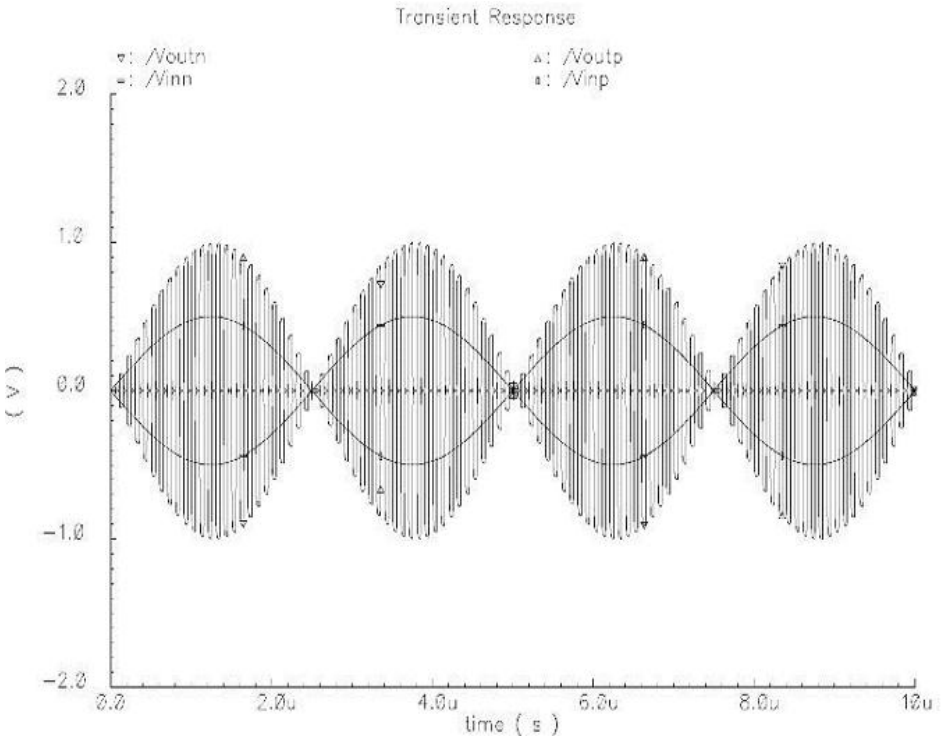


Figure 5.16: Gain 2 Stage Result.

connected to the first stage, in order to generate a random signal. From each stage's digital output, the final digital output corresponds to the input signal. Figures 5.17-20 show the select signal output results for the various modes of the pipeline ADC.

Figures 5.21-23 show the synthesis results of the digital block for scheduling. This is done with the Synopsys design analyzer synthesis tool. Figure 5.21 is the top level synthesis block of control logic, input is the clock and operation modes, so depending on the mode, selected signals are defined for each stage, this block controls the pipeline ADC and performs the scheduling

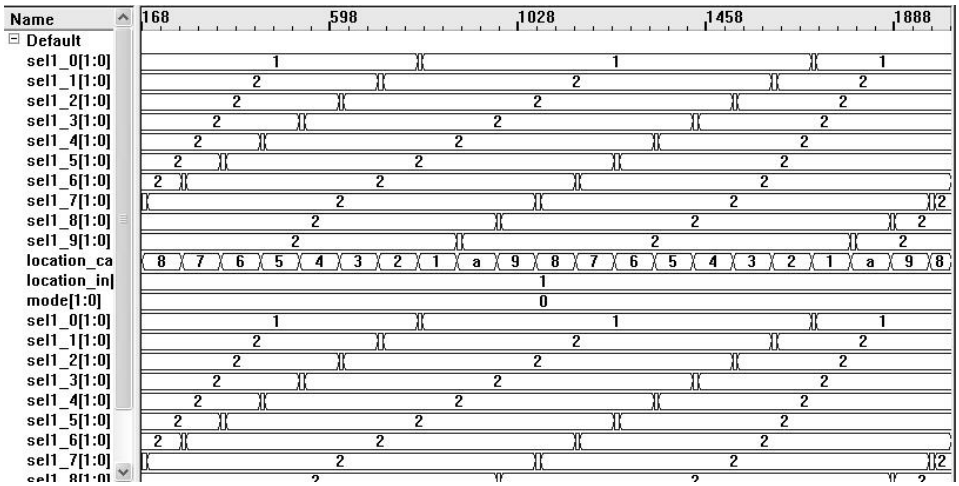


Figure 5.17: Simulation of Digital Logic (Normal Mode).

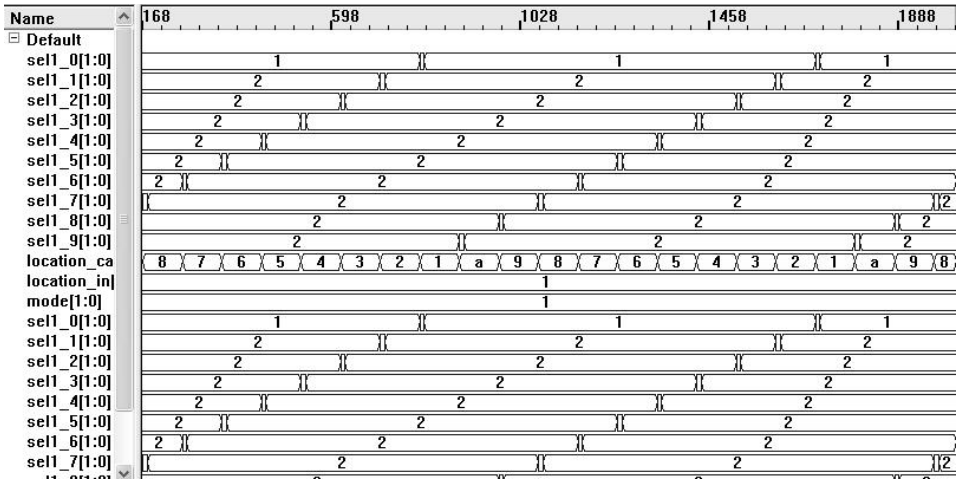


Figure 5.18: Simulation of Digital Logic (Calibration Mode).

of calibration and testing in the background.

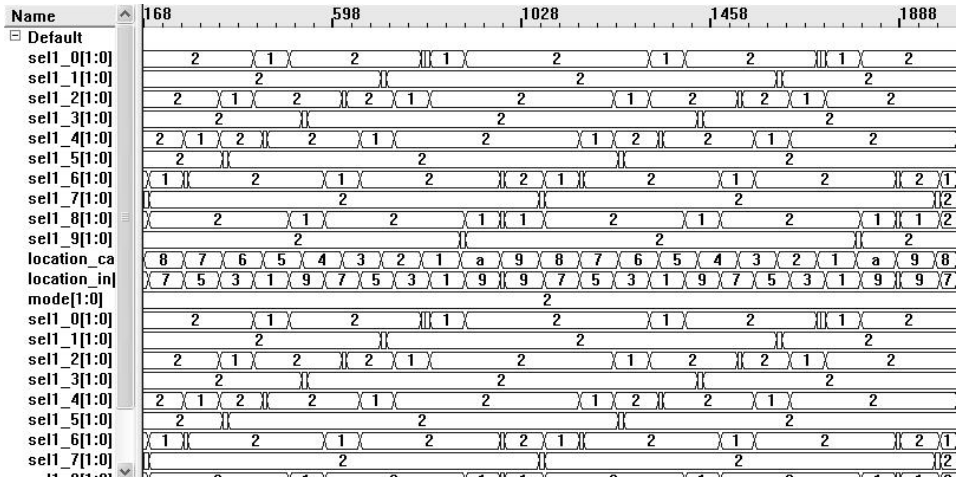


Figure 5.19: Simulation of Digital Logic (Testing Mode).

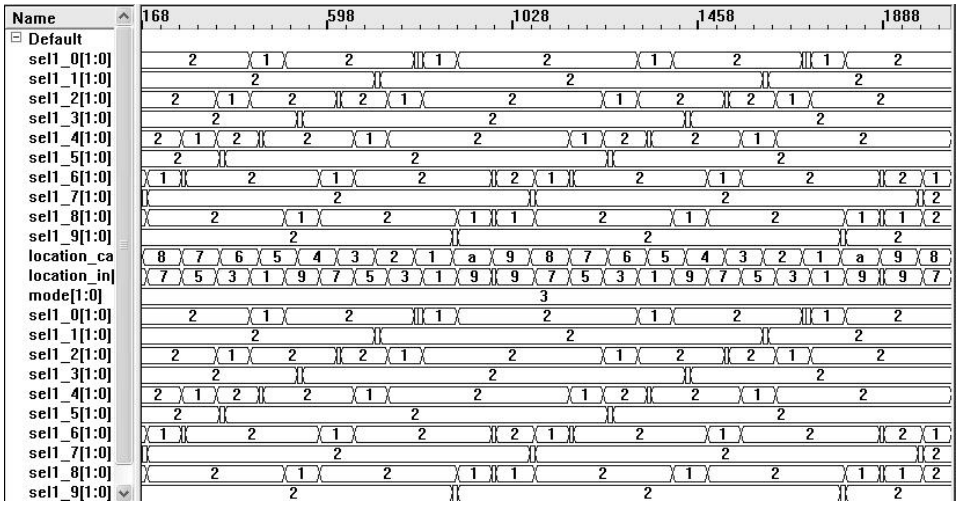


Figure 5.20: Simulation of Digital Logic.

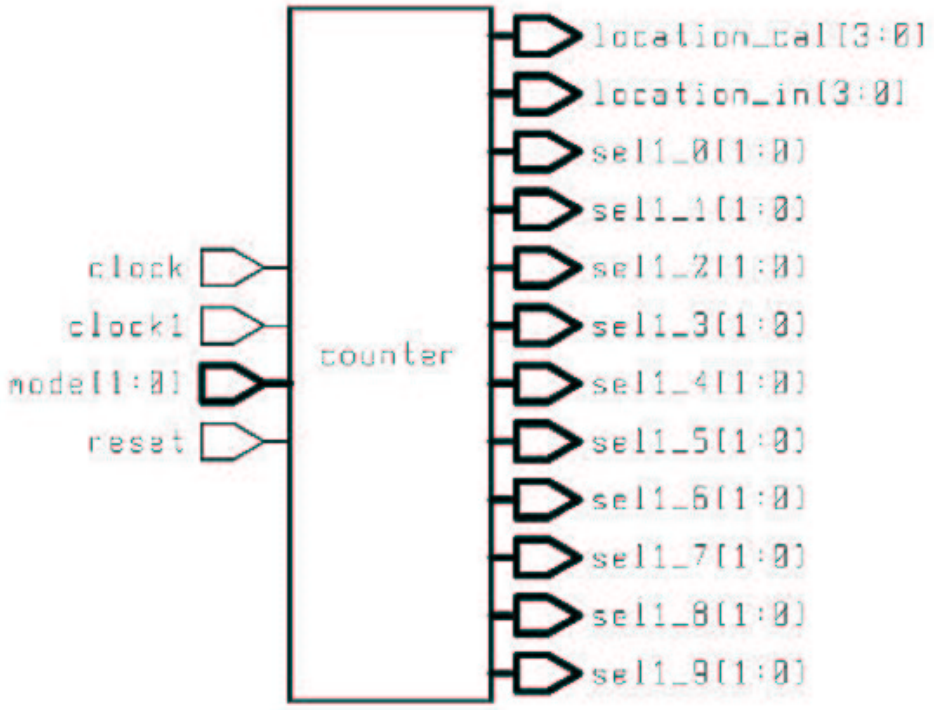


Figure 5.21: Digital Block of Scheduled Calibration Technique.

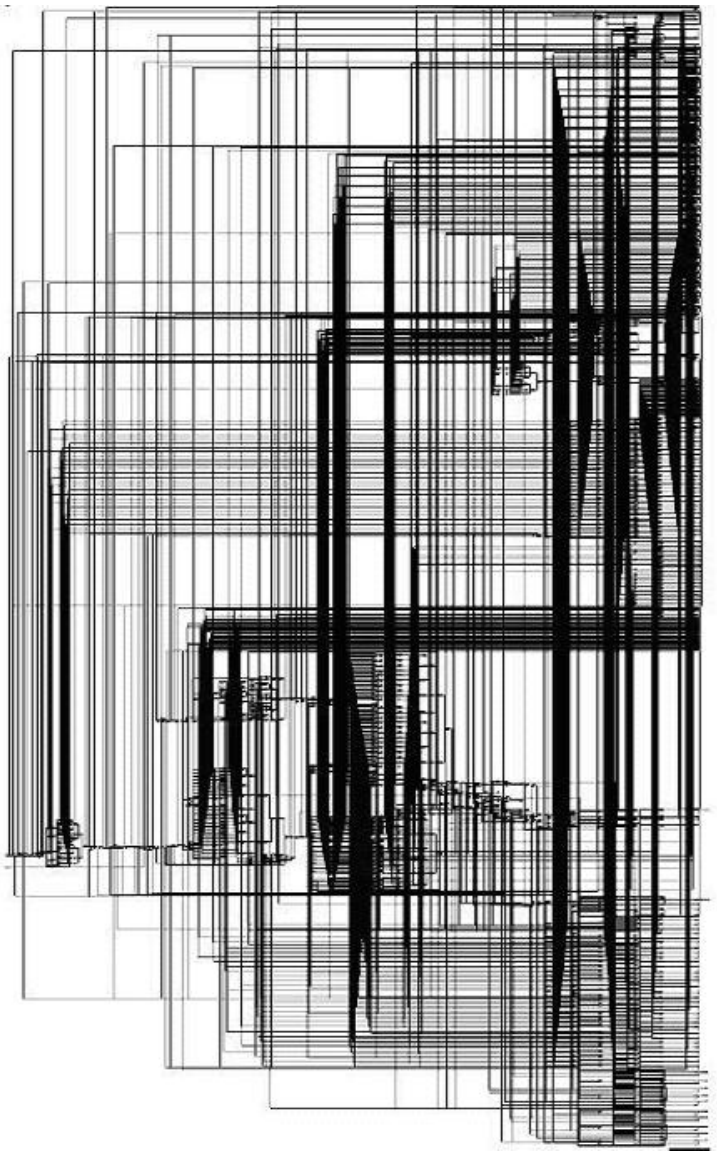


Figure 5.22: Synthesis of the Digital Block.

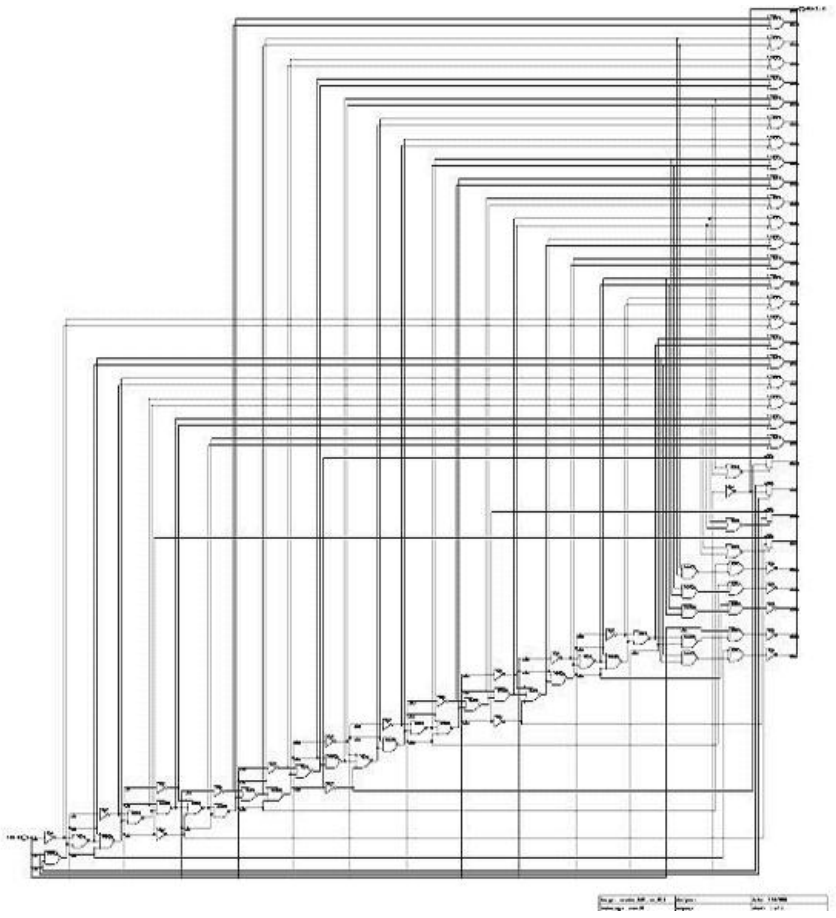


Figure 5.23: Synthesis of the Counter Block.

Chapter 6

Conclusion and Future Research

6.1 Conclusion

In this research, a new digital background calibration technique with two redundant stages is proposed. Due to the redundant stages, calibration cycles can be scheduled to the pipeline stages during normal operation. The basic building blocks are the same as the building blocks in a normal pipeline ADC and no extra design time is required for dedicated calibration ADCs or DACs. This technique can calibrate all the gain errors, offset errors and the non-linearity errors of the ADC except for the front-end S/H. When compared to the normal digital calibrated pipeline ADC, the digital hardware complexity is slightly increased. When compared to other background calibration techniques, it represents a compromise solution between with and without additional calibration converters. It is also suitable for converting high frequency input signals since there is nothing inherent in the algorithm that will degrade the performance for high input frequencies. A self-generated random signal based on the congruential mapping found in pipeline A/D converters is used as the test signal stimulus for histogram test. Almost no extra analog components are required for this random signal generation. The testing technique can be extended to in-field background verification if the converter is calibrated using

skip-and-fill background calibration method. With a sufficient number of sample data the results are obtained with a precise ramp input signal histogram test. In Chapter 3, the behavior simulation with Matlab verifies the efficacy of these techniques.

Chapter 4 shows simulation results for many blocks of the ADC needed to implement the real circuit. The pipeline ADC is designed to achieve 50 MHz, 12-bits with a 1.5 bit per stage architecture in the TSMC 0.25μm CMOS process. Each stage contains a switched-opamp with high-gain and large output signal swing. A modified two-stage folded-cascode opamp is used. This opamp has one extra transistor in the input stage, and this transistor takes care of the common-mode feedback. Using two stages for the main amplifier, a large output signal swing can be achieved. PMOS and NMOS gain boosting amplifiers are used to get higher DC gain.

The digital block, which generates the select signal of each stage for calibration and testing, is designed using Verilog HDL. Depending on the operation mode, the multiplexer located in front of each stage selects one of the two signals. When the previous signal is selected, the operation is normal mode, but when the front-end S/H output is selected, then this stage becomes the first (i.e., input) stage. Depending on the select signal generated by the digital logic, each stage generates a digital output. The digital calibration algorithm is simulated with Matlab. The schematic simulation gives the digital output, with this digital output the INL and DNL is calculated using Matlab. The INL and DNL result is worse than the ideal Matlab simulation, but

using this technique, the pipeline ADC can be calibrated and tested in the background, so these techniques are expanded to work in real time without interrupting the normal operation of the converter.

6.2 Future Research

In the future, both digital and analog circuits will clearly need a finite amount of voltage and a minimum amount of margin is fundamentally necessary. High supply voltages bring several issues in the integrated circuits, such as thin gate oxide reliability issue, hot carrier effect, especially when the technology is scaled down. Reduction of system power consumption and extension of battery life are also of great interest now. While using low supply voltage can mitigate these issues and reduce the system power, many analog circuits suffer performance degradation or cease to function at low supply voltages. At low supply voltages, to achieve comparable performance with traditional circuits sometimes requires putting more current into the analog circuits, which is not favorable from the point of power dissipation. Careful design at the architectural and circuit level can minimize power consumption without affecting the overall system performance.

Due to current leakage considerations, a threshold voltage less than 0.4V is very difficult, but it is clear that the operating voltages for CMOS technology will be reduced much faster than historical trends. The main drivers of this trend are the need for long-term product reliability and low power, digital operation. Because integrated analog circuitry is becoming a

smaller, but fundamentally necessary, portion of die area, it becomes more difficult to justify modifying the technology for analog needs. Therefore, the analog circuits must be modified to operate on low voltage. Furthermore, it is important that the MOS devices are not unduly stressed in the process, which would degrade product lifetime. So lowering the supply voltage causes many difficulties in designing switched-capacitor circuits, Further research should be conducted to solve these problems.

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